物理设计

iEDA实践

李兴权

iEDA

iEDA

01 Introduction

02 iEDA

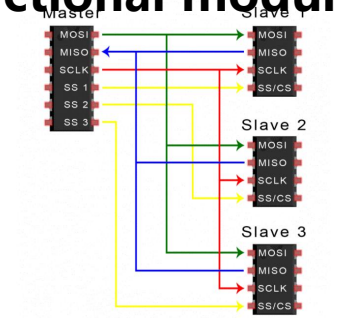
03 iEDA Design Chip

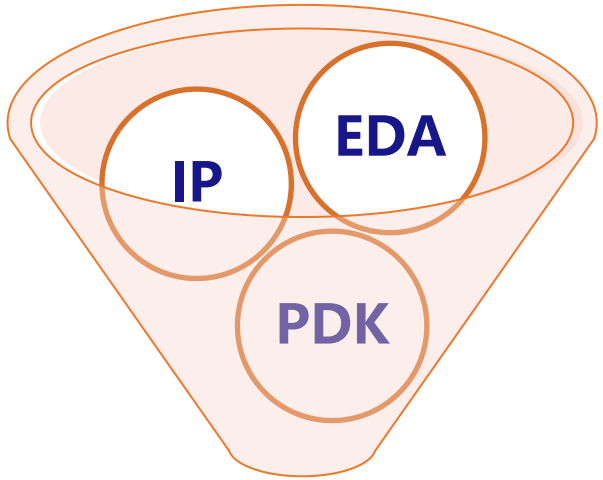
04 iEDA Community

Chip Design Elements

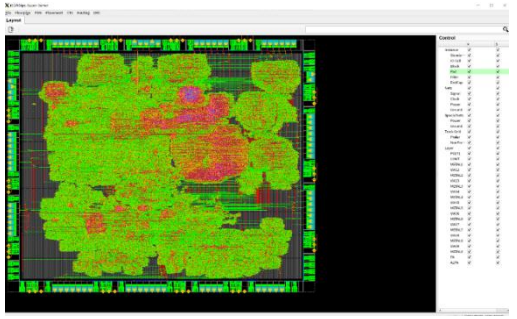
iEDA

IP: Intellectual Property
Functional module

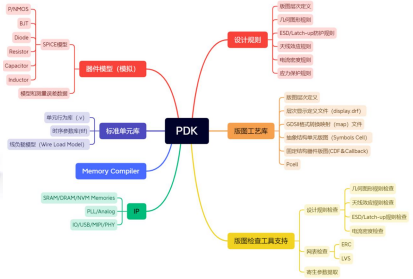




EDA: Electronic design automation software (tool)

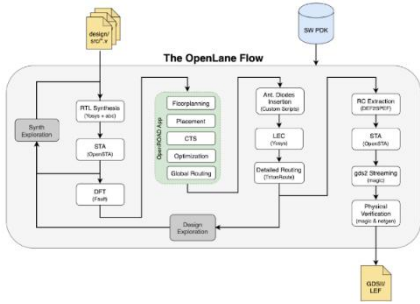


PDK: Process design kits from foundary



Flow

Flow: Chip design flow config and script

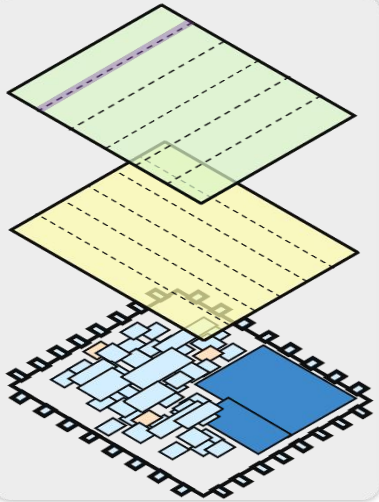


Physical Design

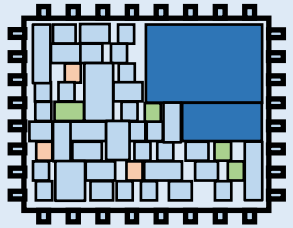
iEDA

- System Specifications
- Architectural Design
- Functional Design
- Logic Synthesis
- Tech Mapping
- **Physical Design**
- Physical Verification
- Sign Off
- Layout Processing
- Fabrication
- Package and Test

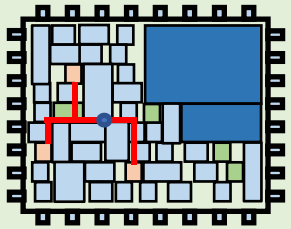
Netlist



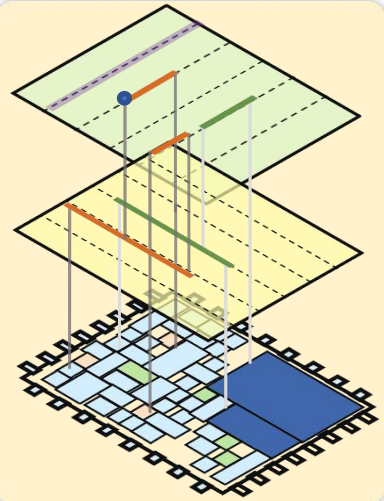
Floorplan: ensure die and core sizes, place IOs, plan macros, plan PDN, place physical cell.



Placement: place std cell into legal position, insert filler, opt timing, power and routability.

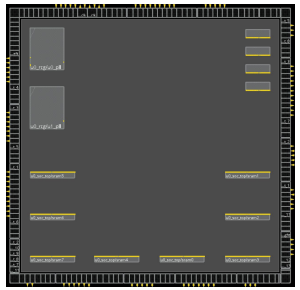


CTS: design clock network, connect FFs, opt skew, latency and power.

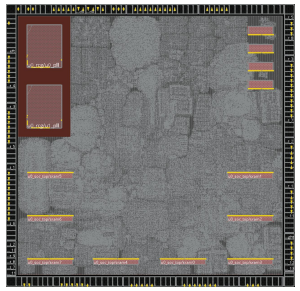


Routing: route net into routing track, opt timing, power and DRC.

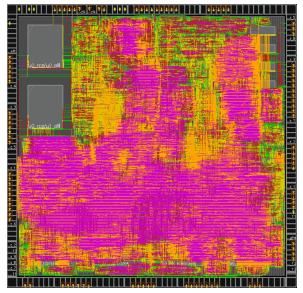
GDS II



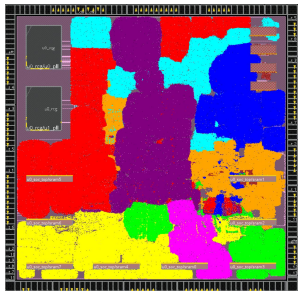
Floorplan



Placement



CTS

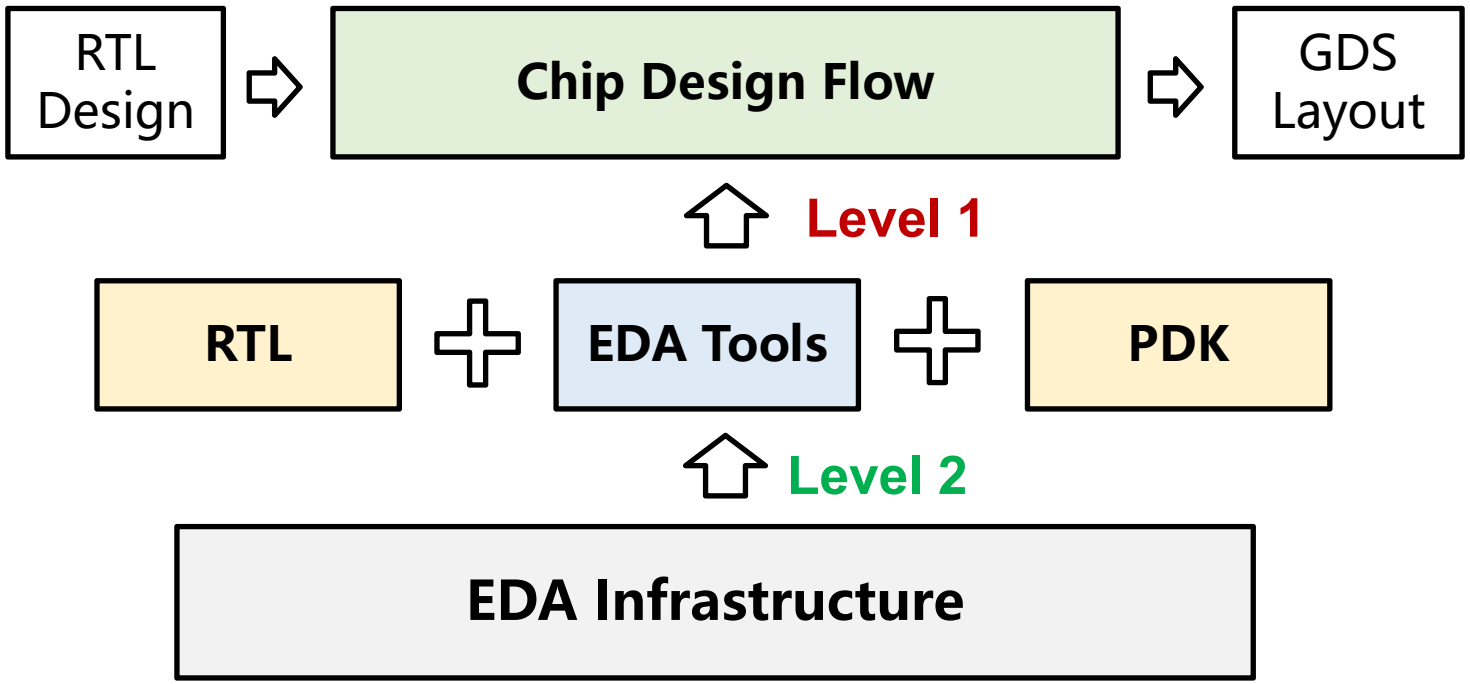


Routing

We Need Infrastructure

iEDA

- **Level 1:** Open-source tools, RTLs, PDKs support chip design
- **Level 2:** Open-source Infrastructure supports EDA development



iEDA

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02 iEDA

03 iEDA Design Chip

04 iEDA Community

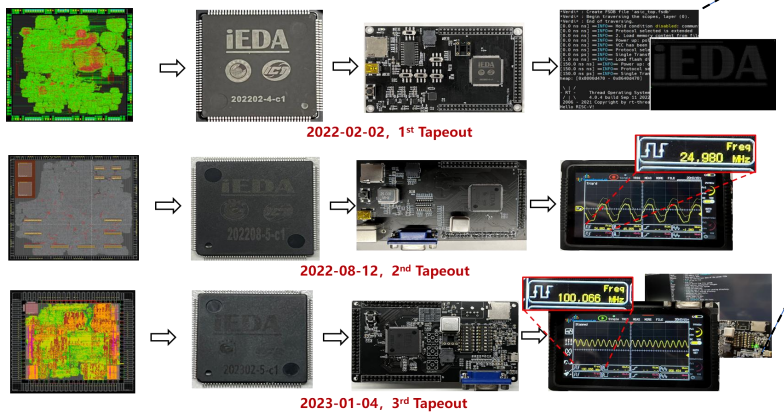
iEDA Overview

- **EDA Infrastructure、EDA Tools、3 times tape-out design by iEDA**
  - **Level 1: Open-source EDA, RTL, PDK, supporting chip design;**
  - **Level 2: Open-source Infrastructure supports EDA development and research**

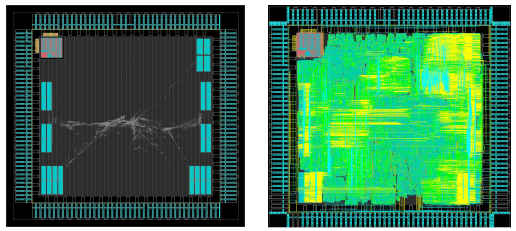
1st Tapeout
- RTL: ysyx03
- PDK: 110nm
- Area: 3mm × 3.5 mm
- Power: dynamic = 48mW, leakage = 7 mW
- Freq.: 25MHz
- Scale: >70万 Gates
- Features: 5 pipeline, Chiplink, UART、SPI、PCB clock, support RT-thread

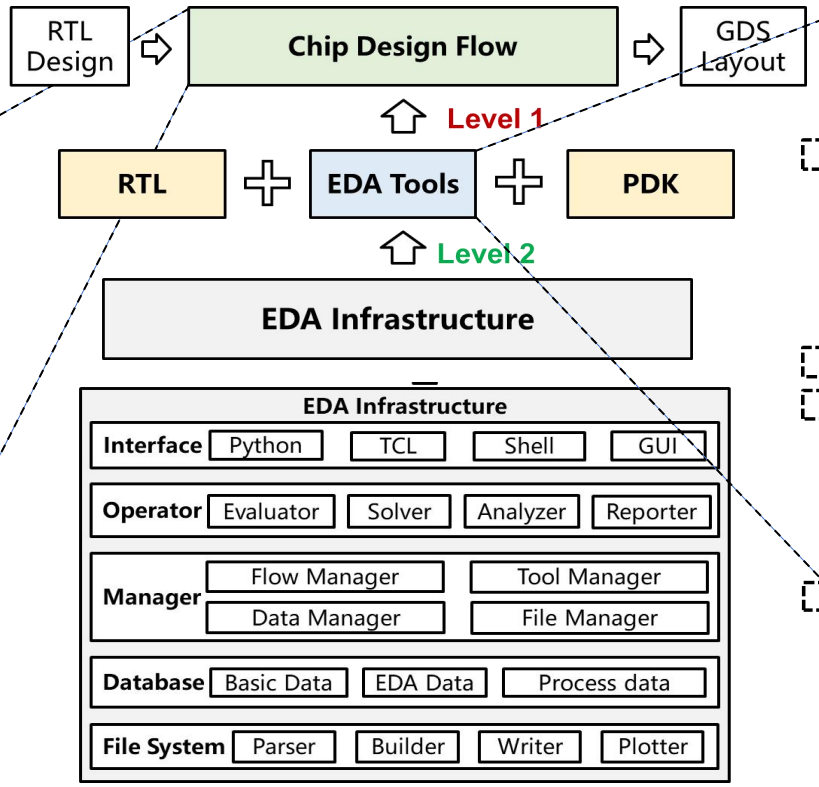
2nd Tapeout
- RTL: ysyx04
- PDK: 110nm
- Area: 4.5mm × 4.5 mm
- Power: dynamic = 343mW, leakage = 21 mW
- Freq.: 25MHz
- Scale: >1.5M Gates
- Features: 11 pipelines with cache, IP: UART、VGA、PS/2、SPI、SDRAM、2 PLLs, support Linux

3rd Tapeout
- RTL: ysyx04
- PDK: 28nm
- Area: 1.5mm × 1.5 mm
- Power: dynamic = 317mW, leakage = 29 mW
- Freq.: 200MHz
- Scale: >1.5M Gates
- Features: 11 pipelines with cache, IP: UART、VGA、PS/2、SPI、SDRAM、2 PLLs, support Linux

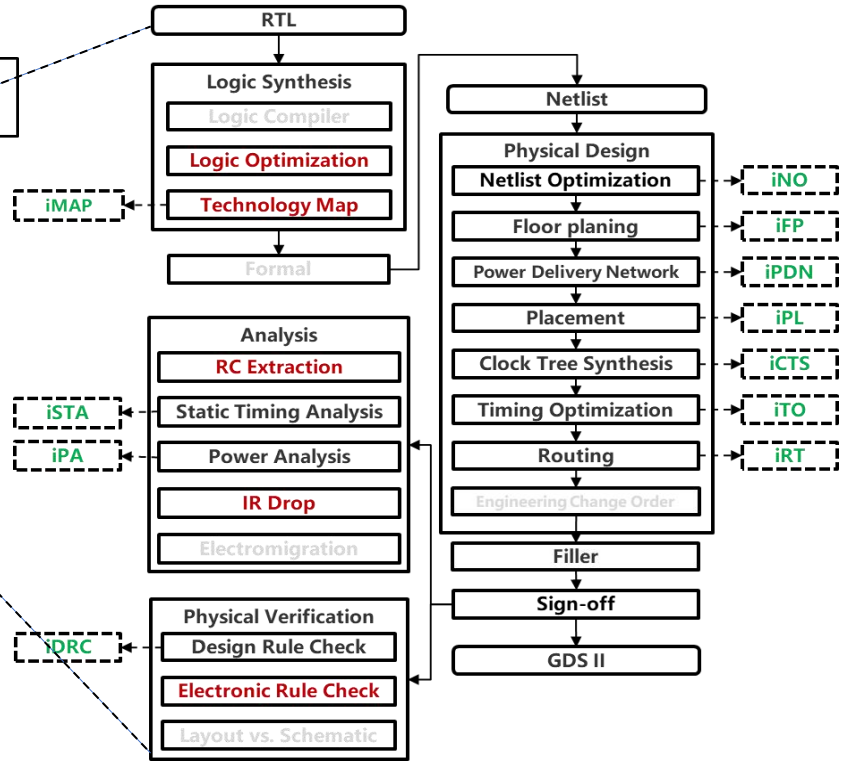


3 times tape-out





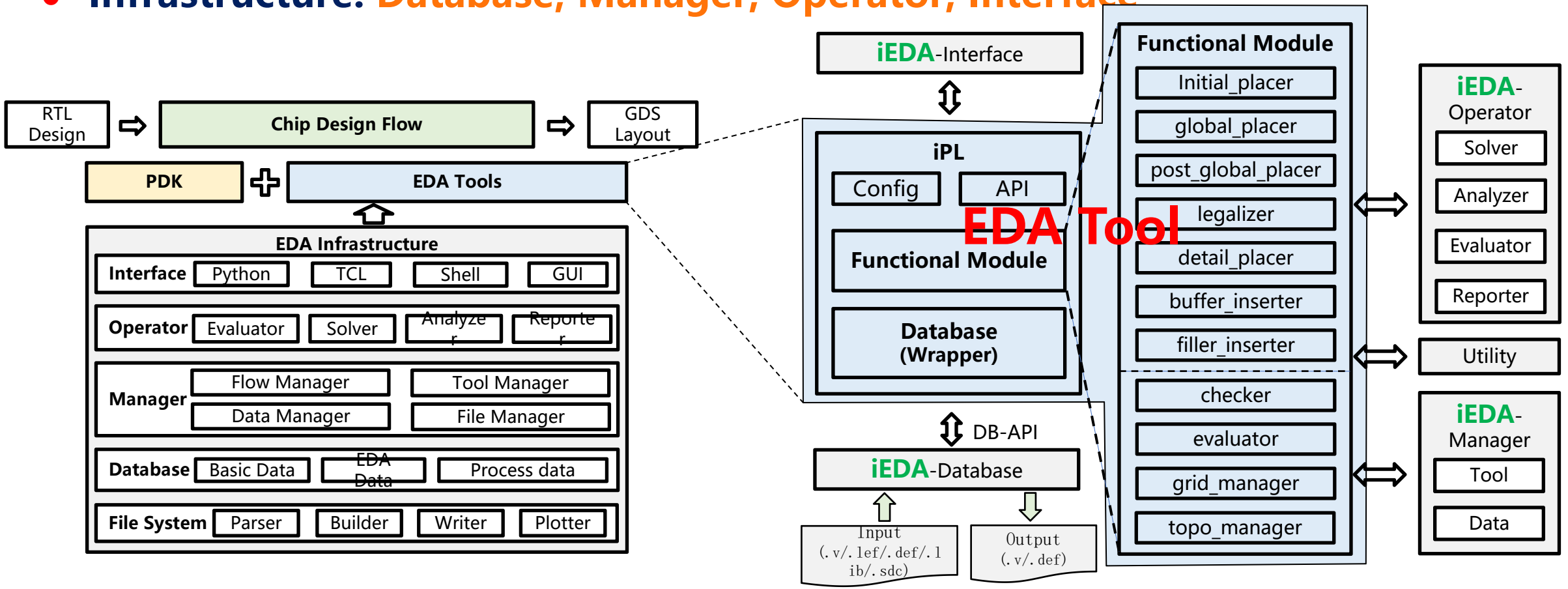
1 EDA infrastructure



11 EDA tools, 200 technologies, 300 K lines codes

iEDA Infra. Support EDA Tool

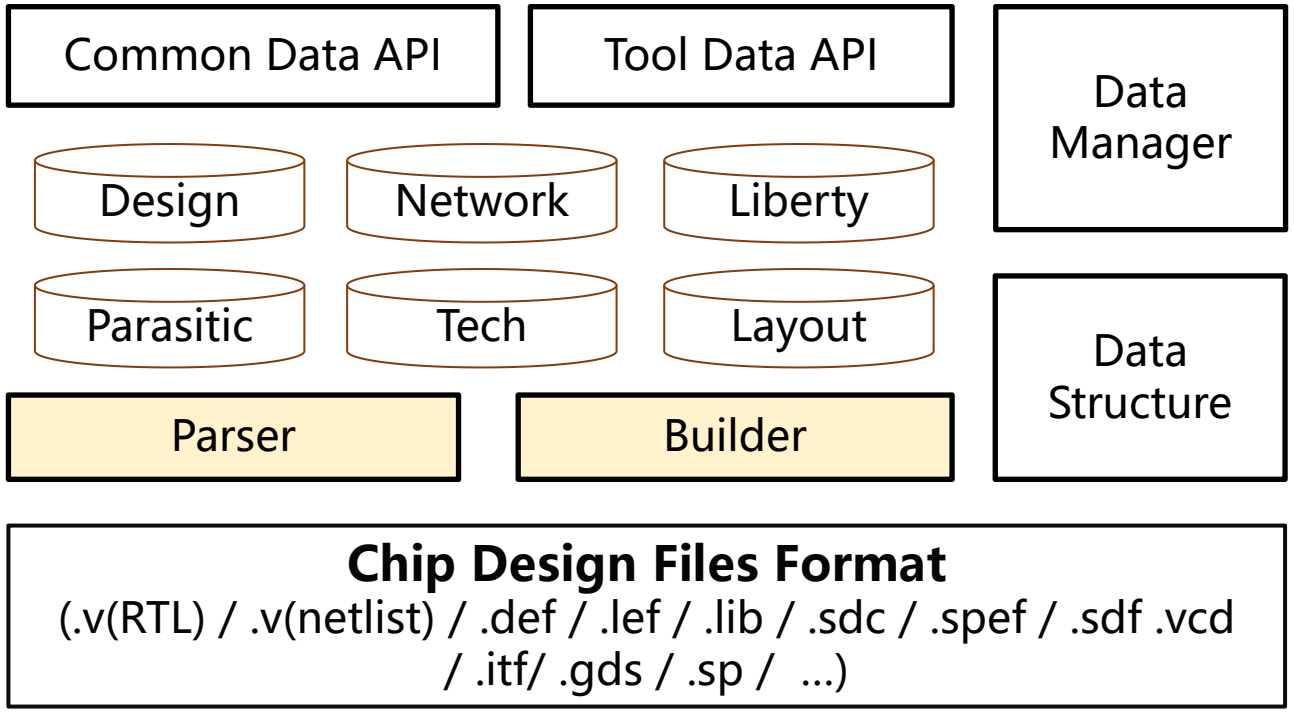
- To fast develop high-quality EDA tool, we need a **S**oftware **D**evelopment **K**it (**SDK**)
- iEDA can be used to support developing EDA tool or algorithm
- **Infrastructure: Database, Manager, Operator, Interface**



Parsers and Database

iEDA

- **Parser: Verilog, SPEF, Liberty, SDF, VCD, SDC, LEF/DEF, ITF, and GDSII**
- **Database: Design, Layout, Tech, Timing, Parasitic, Network**



Managers

iEDA

Platform Manager

Data

- Config
- ChipData
- Interactive
- Proc Data
- ...

Flows

- Initialize
- Input
- Process
- Output

Tools

- Floorplan
- NetOpt
- Placement
- CTS
- TimingOpt
- Legalization
- Routing
- Filler
- DRC
- ...

Features

- Summary
- Density
- Wire Length
- Congestion
- Profiles
- ...

Reports

- Statistic
- Evaluation
- Flow Results
- Timing
- DRC
- ...

Files

- Config
- Design
- Procedure
- Serialize
- ...

Interfaces

TCL

- Flows
- DB
- Tools
- Evaluation
- Features
- Reports
- GUI

```
├── tcl_config
├── tcl_contest
├── tcl_eval
├── tcl_feature
├── tcl_flow
├── tcl_gui
├── tcl_icts
├── tcl_idb
├── tcl_idrc
├── tcl_ifp
├── tcl_ino
├── tcl_instance
├── tcl_ipdn
├── tcl_ipl
├── tcl_ipw
├── tcl_irt
├── tcl_ista
├── tcl_ito
├── tcl_report
└── tcl_util
```

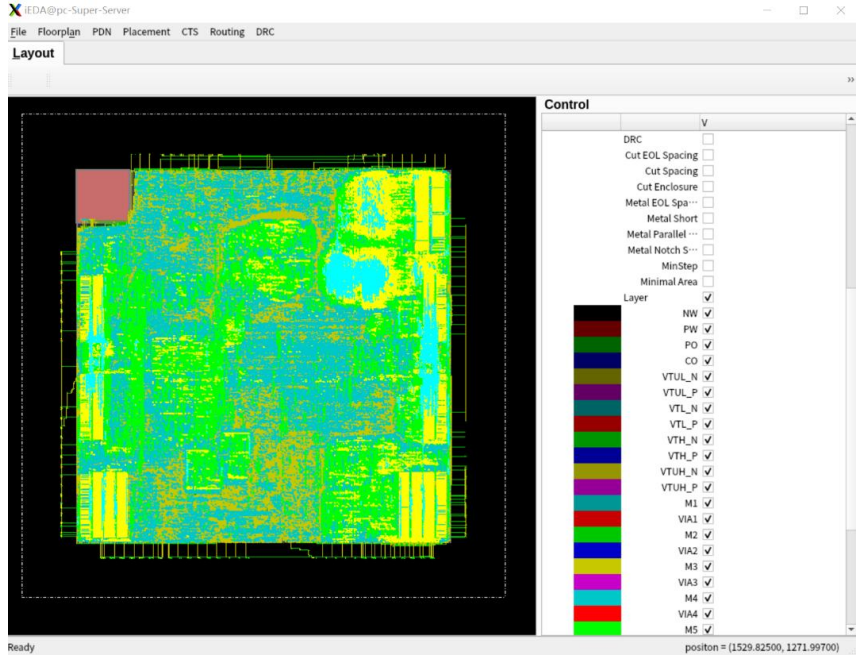
Python

- Flows
- DB
- Tools
- Evaluation
- Features
- Reports

```
├── py_config
├── py_eval
├── py_feature
├── py_flow
├── py_icts
├── py_idb
├── py_idrc
├── py_ifp
├── py_imp
├── py_ino
├── py_instance
├── py_ipdn
├── py_ipl
├── py_ipw
├── py_irt
├── py_ista
├── py_ito
└── py_report
```

GUI

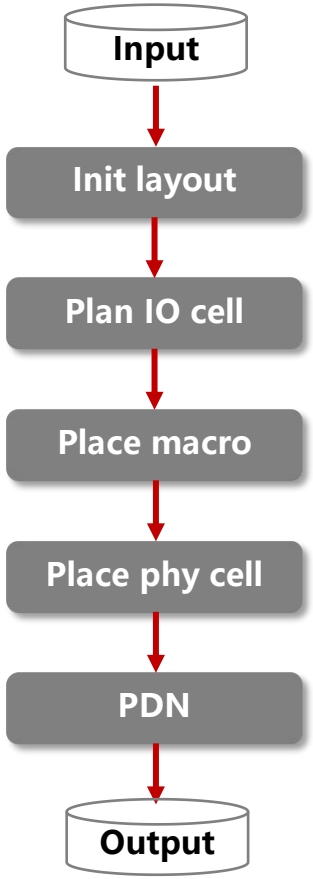
- File Operation
- Layout View
- Layers Control
- Shape Setting
- Instance Options
- Net Options
- PDN Options
- Track Grid
- DRC View
- Clock Tree View



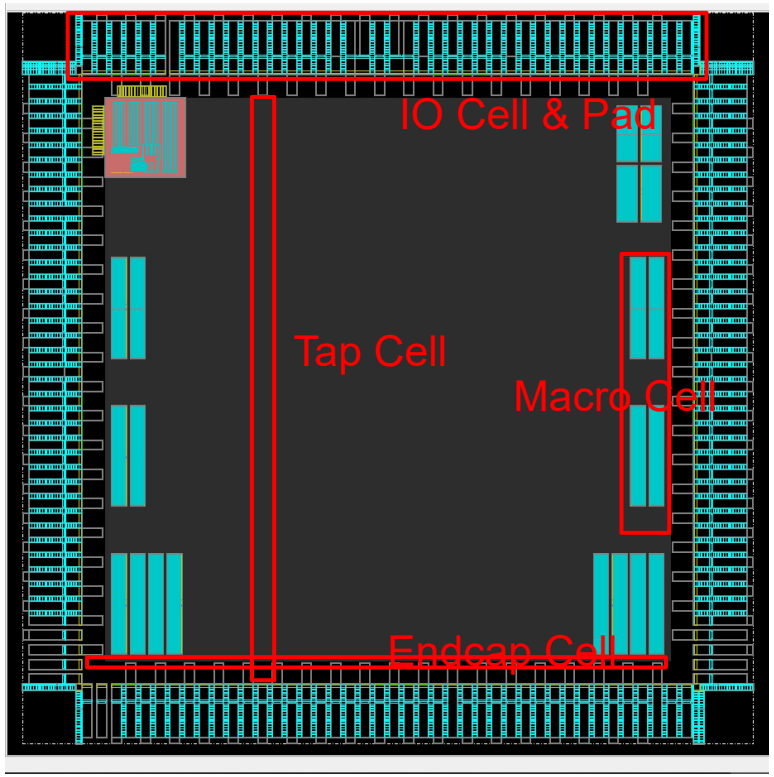
Floorplan (iFP) & Power Delivery Network (iPDN)

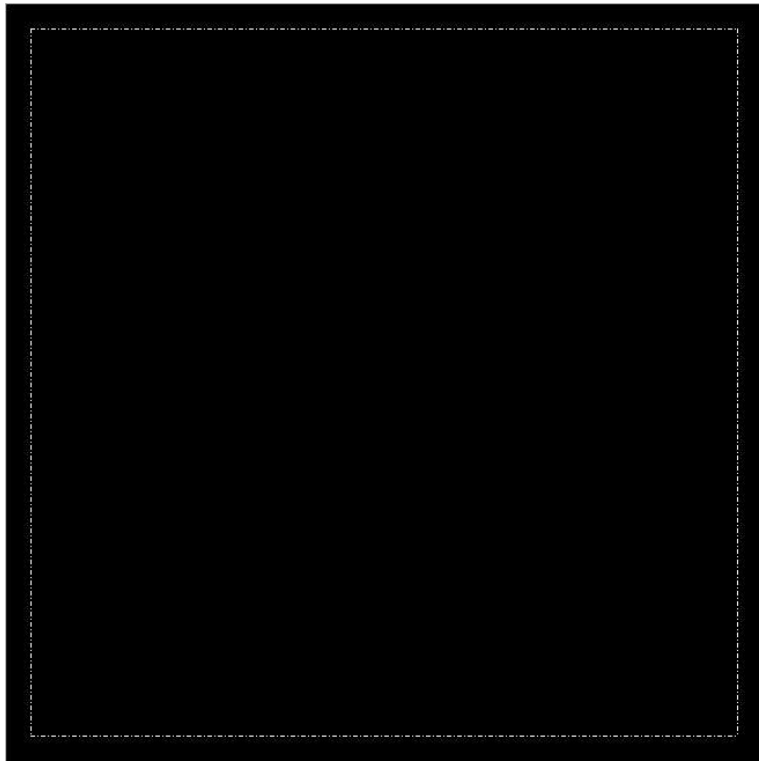
iEDA

Flow



Key Metrics	Data
DIE Area	1.5 × 1.5 mm^2
DIE Utili	0.166554
Core Area	1.16 × 1.15 cm^2
Core Utili	0.279541
#IO Pin	110
#Instance	297504
#Net	311869
Pin	**pin（>= 32）= 2893**
PDN	M1、M2、M7、M8、M9、AP

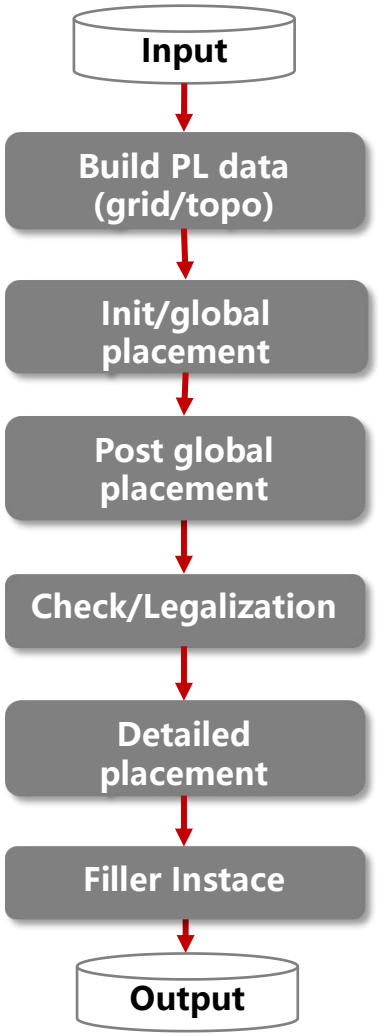


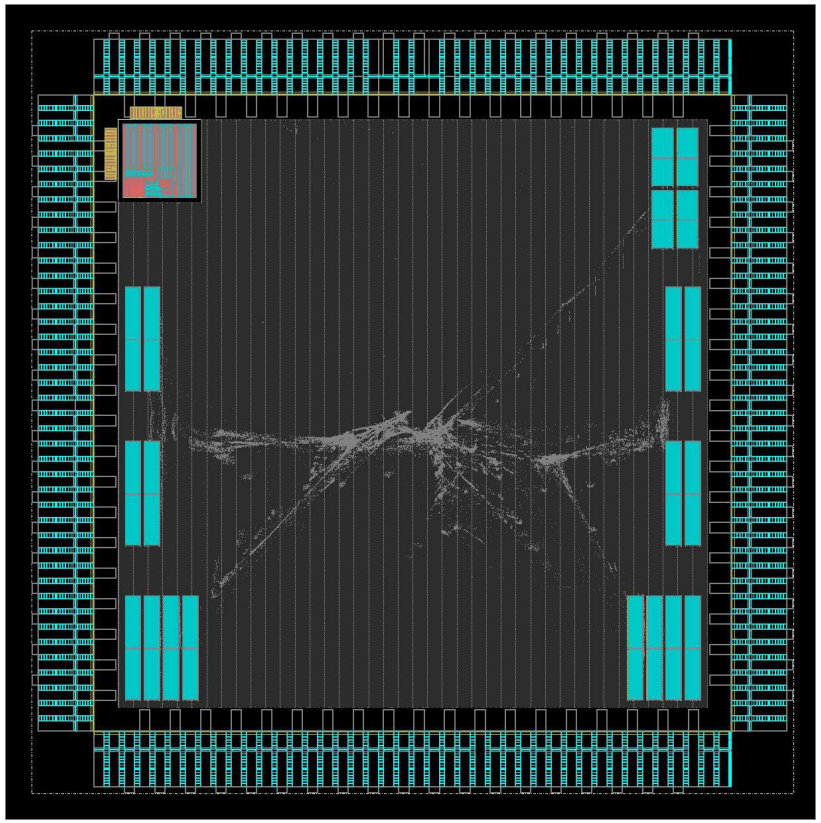


Placement (iPL)

iEDA

Flow





■ Min Wirelength Model

$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \ \ \forall b \in B$$

where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

$\boldsymbol{W(v)}$

$$HPWL_{ex}(\mathbf{v}) = \max_{i,j \in e} |x_i - x_j|$$

$$LSE_{ex} = \gamma \left(\ln \left(\sum_{i \in e} \exp\left(\frac{x_i}{\gamma} \right) \right) + \ln \left(\sum_{i \in e} \exp\left(\frac{-x_i}{\gamma} \right) \right) \right)$$

$\boldsymbol{\rho_b(v)}$

$$D(\boldsymbol{v}) = \frac{1}{2} \sum_{v \in V} D_i(x,y) = \frac{1}{2} \sum_{v \in V} q_i \psi_i(x,y)$$

$$\begin{cases} \nabla \cdot \nabla \psi(x,y) = -\rho(x,y), \\ \hat{\boldsymbol{n}} \cdot \psi(x,y) = \mathbf{0}, \ \ (x,y) \in \partial R \\ \iint_R \rho(x,y) = \iint_R \psi(x,y) = 0. \end{cases}$$

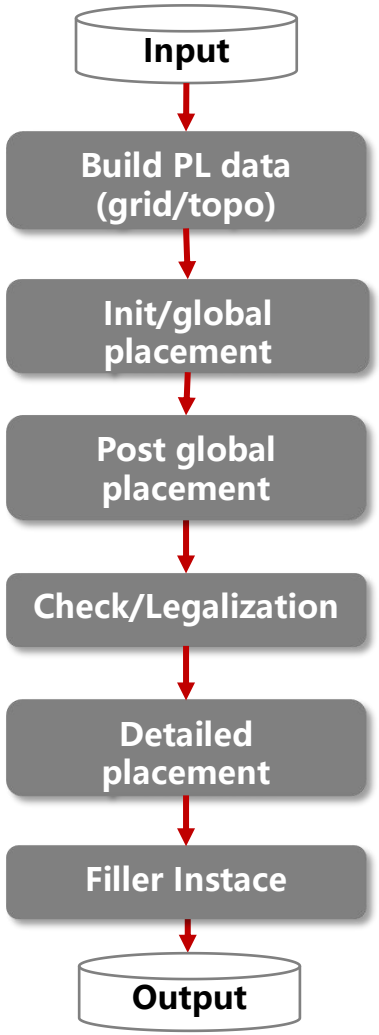
$$\min_{\boldsymbol{v}} \quad f(v) = W(\boldsymbol{v}) + \lambda \sum_{\forall b \in B} \boldsymbol{\rho_b}(\boldsymbol{v})$$

- **Nesterov Method or** Conjugate Gradient

Placement (iPL)

iEDA

Flow



Key parameter config	
Input	iFP.def, iFP.v
output	iPL_result.def, iPL.v
is_max_length_opt	Whether to enable max wirelength optimization
max_length_constraint	set max wirelength constraint
is_timing_aware_mode	Whether to enable timing opt
ignore_net_degree	ignore net whose pin number > k
num_threads	set number of CPU thread
[BUFFER] max_buffer_num	Set the number of using max buffer
[BUFFER] buffer_type	Set available buffer name
[GP-Wirelength] min_wirelength_force_bar	Control wirelength range
[GP-Density] target_density	Set target density
[GP-Density] bin_cnt_x	Set the number of horizontal Bin
[GP-Density] bin_cnt_y	Set the number of vertical Bin
[LG] global_right_padding	Set instance spacing (/site)
[DP] global_right_padding	Set instance spacing (/site)
[Filler] min_filler_width	Set min width of filler (/site)

Basic Summary

summary_report.txt

scripts > sky130 > result > pl > report > summary_report.txt

```
Generate the report at 2023-08-15T15:10:33
+----------------------+----------+
| Base Info            | Value    |
+----------------------+----------+
| Design               | gcd      |
| Utilization          | 0.098599 |
| Site Num             | 78 * 542 |
| Instances Count      | 795      |
| - Macro Count        | 0        |
| - StdCell Count      | 795      |
| -- FlipFlop Count    | 34       |
| -- Clock Buffer Count| 0        |
| -- Normal Logic Count| 761      |
| Nets Count           | 675      |
| - Signal Net Count   | 674      |
| - Clock Net Count    | 1        |
| - Reset Net Count    | 0        |
| - Other Net Count    | 0        |
+----------------------+----------+

+---------------------------------+-------+
| Violation Info                  | Value |
+---------------------------------+-------+
| Core Range Violated Count       | 0     |
| Row/Site Alignment Violated Count | 0   |
| Power Alignment Violated Count  | 0     |
| Overlap Violated Count          | 0     |
+---------------------------------+-------+

+-----------------------------------+----------+
| Wirelength Info                   | Value    |
+-----------------------------------+----------+
| Total HPWL                        | 14402289 |
| Max HPWL                          | 328905   |
| Total STWL                        | 15057480 |
| Max STWL                          | 512025   |
| LongNet HPWL (Exceed 1000000) Count | 0      |
+-----------------------------------+----------+

+------------------+----------+
| Bin Density Info | Value    |
+------------------+----------+
| Peak BinDensity  | 1.000000 |
+------------------+----------+

+------------------+-----------+-----------+-----------+-----------+
| Clock Timing Info | Early WNS | Early TNS | Late WNS  | Late TNS  |
+------------------+-----------+-----------+-----------+-----------+
| core_clock       | 0.000000  | 0.000000  | -0.194720 | -2.818471 |
+------------------+-----------+-----------+-----------+-----------+

+----------------------------+-----------+
| Congestion Info            |           |
+----------------------------+-----------+
| Average Congestion of Edges | 0.537355 |
| Total Overflow             | 53.000000 |
| Maximal Overflow           | 18.000000 |
+----------------------------+-----------+
```

Wirelength
wl_detail_report.txt

Instance density

Timing

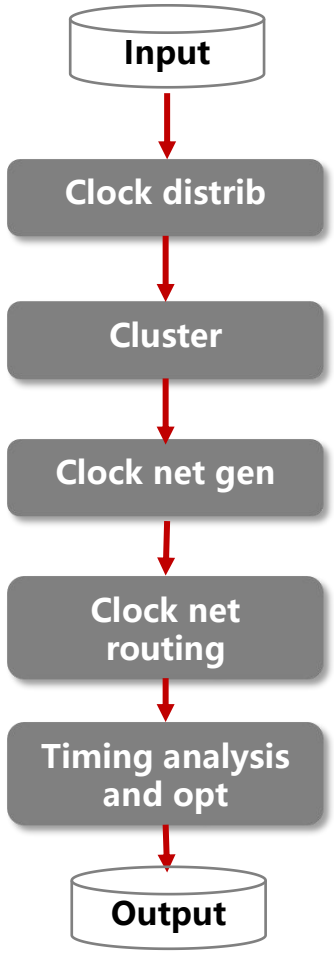
Congestion

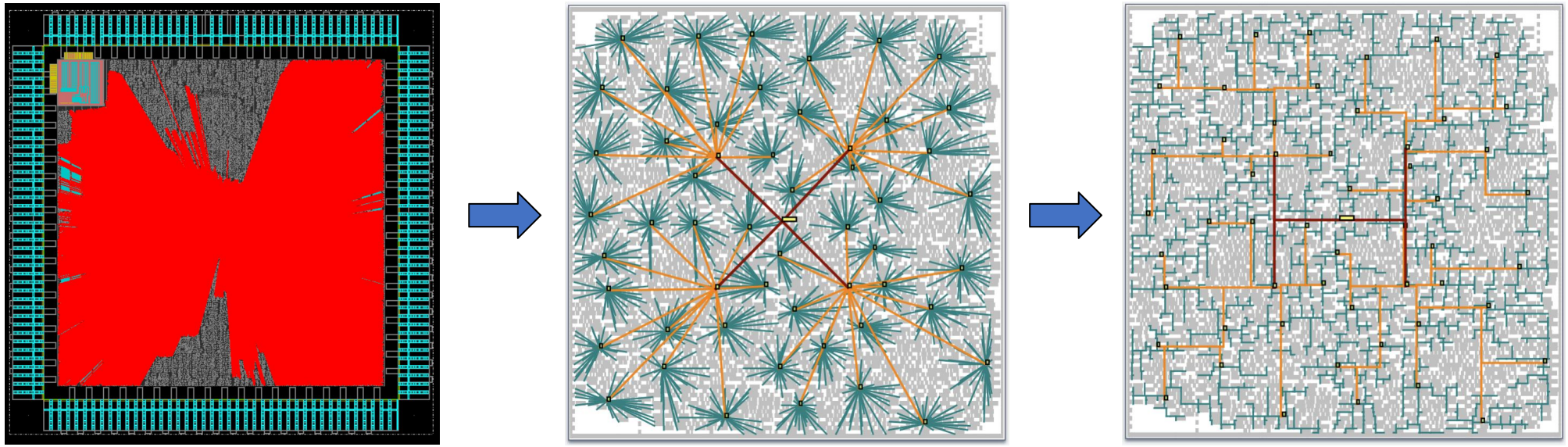
Design rule violation
violation_detail_report.txt

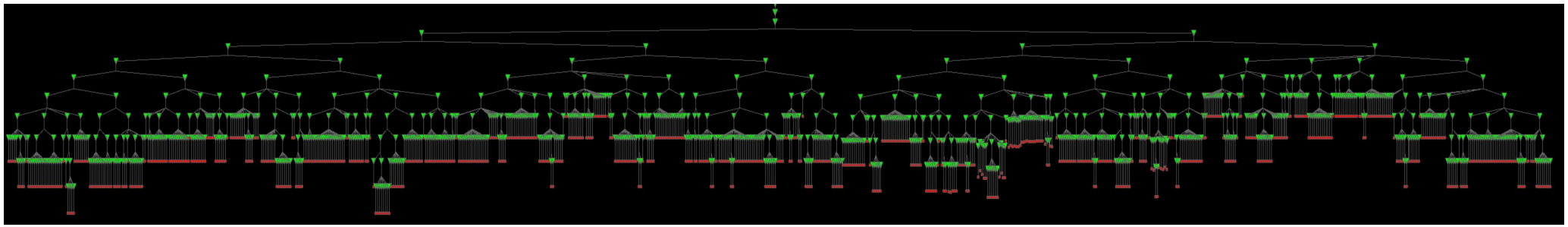
Clock Tree Synthesis (iCTS)

iEDA

Flow



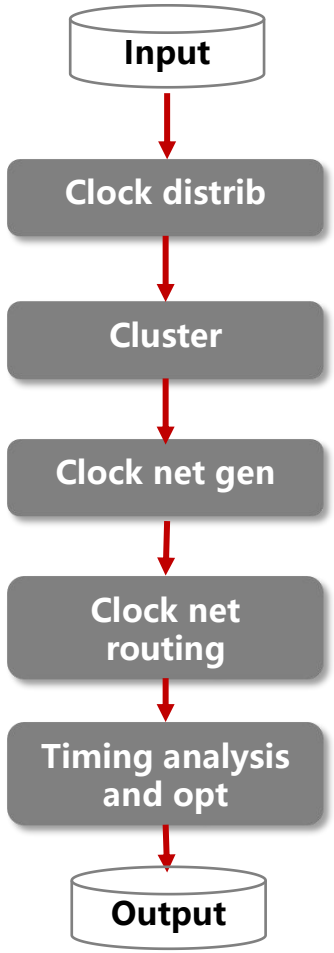




Clock Tree Synthesis (iCTS)

iEDA

Flow



Timing

- Latency (max delay)
- Skew

Level	Inst Num	Min Skew	Max Skew	Avg Skew	Violation
1	1210	6.62388e-05	0.0145301	0.00105275	0
2	204	0.000406356	0.0278176	0.00972537	0
3	80	0.0042316	0.0411625	0.0190886	0
4	41	0.00690457	0.0566811	0.0323446	0
5	22	0.0261657	0.0760005	0.0524973	0
6	13	0.0261657	0.0799602	0.0623044	0
7	7	0.0261657	0.08	0.0669329	0
8	4	0.0603809	0.08	0.0743834	0
9	2	0.0799208	0.08	0.0799604	0
10	1	0.08	0.08	0.08	0

Level	Inst Num	Min Delay	Max Delay	Avg Delay	Violation
1	1210	0.000237424	0.0432362	0.00143337	None
2	204	0.0518461	0.0983796	0.0688073	None
3	80	0.119261	0.174637	0.145464	None
4	41	0.187633	0.255905	0.219663	None
5	22	0.250207	0.319777	0.294133	None
6	13	0.324988	0.400232	0.365337	None
7	7	0.405067	0.452041	0.435055	None
8	4	0.500763	0.549897	0.522962	None
9	2	0.573994	0.578742	0.576368	None
10	1	0.608399	0.608399	0.608399	None

Power

- Buffering
- Wirelength

Type	Wire Length
Top	161.021
Trunk	2255.200
Leaf	9267.600
Total	11683.821
Max net length	232.360

Type	HP Wire Length
Top	161.021
Trunk	1347.840
Leaf	3871.380
Total	5380.241
Max net length	161.021

Name	Type	Inst Count	Inst Area (um^2)
CKBD12BWP35P140	Buffer	45	96.39
CKBD16BWP35P140	Buffer	8	22.176
CKBD20BWP35P140	Buffer	12	40.824
CKBD24BWP35P140	Buffer	63	254.016
CKBD4BWP35P140	Buffer	1082	954.324
CKBD6BWP35P140	Buffer	1129	1280.29
CKBD8BWP35P140	Buffer	81	122.472

Violation

- Fanout
- Capacitance
- Slew (transition)

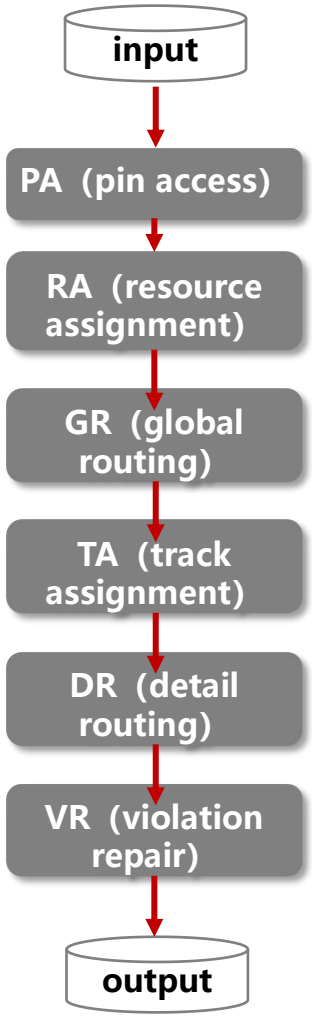
Level	Inst Num	Min Slew	Max Slew	Avg Slew	Violation
1	1210	0.0355823	0.0881141	0.0564704	970
2	204	0.0342527	0.0938317	0.0559007	134
3	80	0.0148774	0.103097	0.0581444	45
4	41	0.00736284	0.102664	0.0516092	20
5	22	0.0175251	0.103516	0.0535373	9
6	13	0.0116574	0.0884235	0.0402797	4
7	7	0.00706415	0.101609	0.0506611	3
8	4	0.015983	0.0220045	0.0188449	0
9	2	0.0259563	0.0286678	0.027312	0
10	1	0	2.22507e-308	0	0

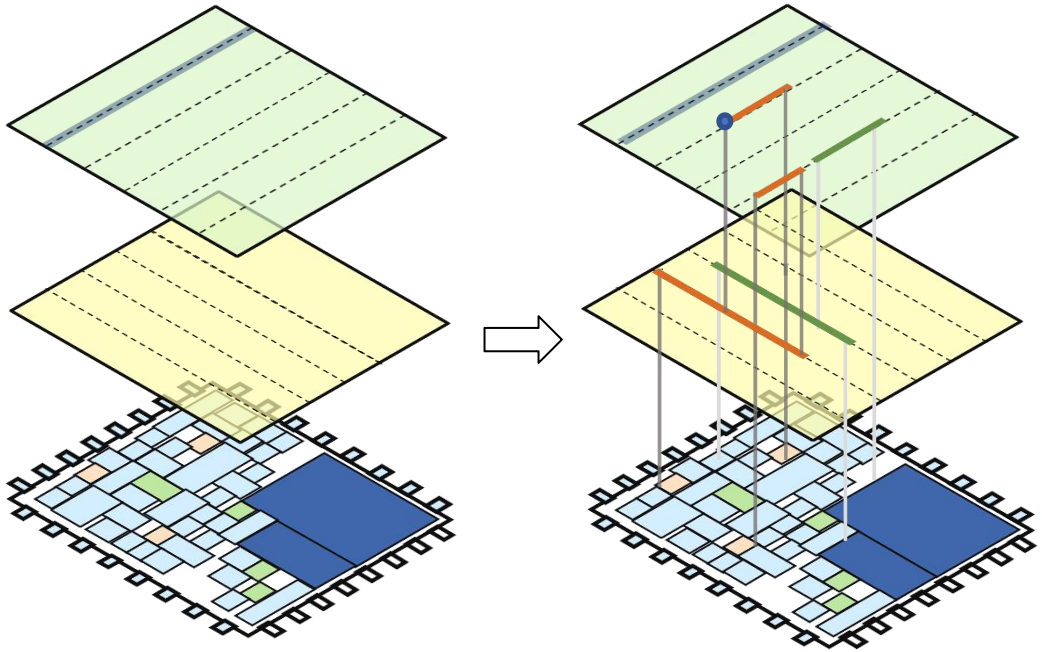
Net / InstPin	MaxTranTime	TranTime	TranSlack	CellPort	Remark
sdram_clk_o					
sdram_clk_o_15397_buf:I	0.800r/0.800f	1.583r/1.494f	-0.783r/-0.694f	CKBD24BWP35P140/I	R
sdram_clk_o					
u0_soc_top/u0_sdram_axi/u_core/U300:ZN	0.800r/0.800f	1.537r/1.446f	-0.737r/-0.646f	INVD1BWP40P140LVT/ZN	R
osc_25m_out_pad					
u0_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
osc_100m_out_pad					
u1_clk:XOUT	5.000r/5.000f	5.704r/9.550f	-0.704r/-4.550f	PDXOEDG_V_G/XOUT	R
clk_hs_peri					
clk_hs_peri_11489_buf:I	0.800r/0.800f	0.850r/0.880f	-0.050r/-0.080f	CKBD24BWP35P140/I	R
u0_rcg/u0_pll_clk					
u0_rcg/u1_lvt_ckmux2hdv4:I1	0.267r/0.267f	0.189r/0.188f	0.078r/0.078f	CKMUX2D4BWP40P140LVT/I1	
u0_rcg/u0_pll_clk					
u0_rcg/u0_pll:FOUTPOSTDIV	0.267r/0.267f	0.000r/0.000f	0.267r/0.267f	PLLTS28HPMLAINT/FOUTPOSTDIV	
clk_core					
clk_core_1724_buf:I	0.800r/0.800f	0.522r/0.533f	0.278r/0.267f	CKBD4BWP35P140/I	
clk_hs_peri					
u0_soc_top/u0_sdram_axi/u_core/U300:I	0.800r/0.800f	0.519r/0.568f	0.281r/0.232f	INVD1BWP40P140LVT/I	
u0_soc_top/n495					
fanout_buf_40:I	0.437r/0.437f	0.098r/0.056f	0.339r/0.381f	BUFFD8BWP30P140LVT/I	

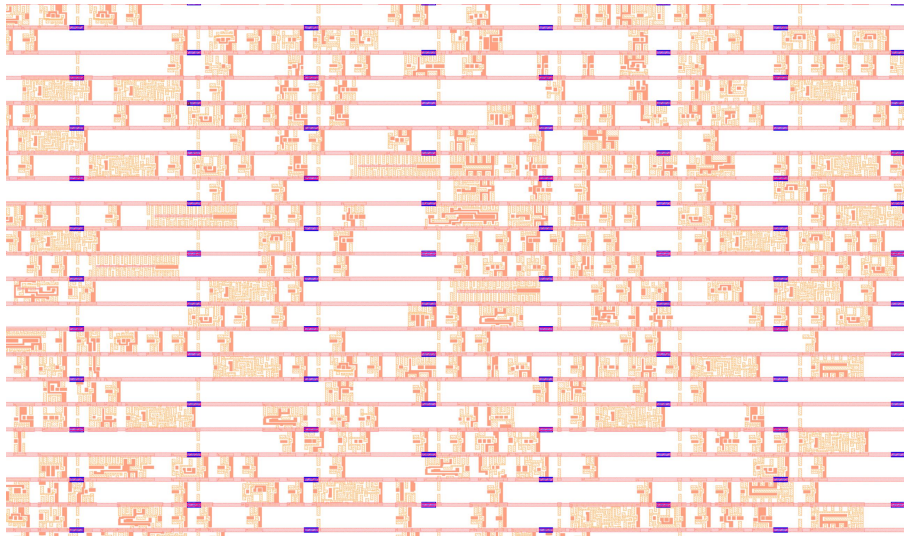
Routing (iRT)

iEDA

Flow





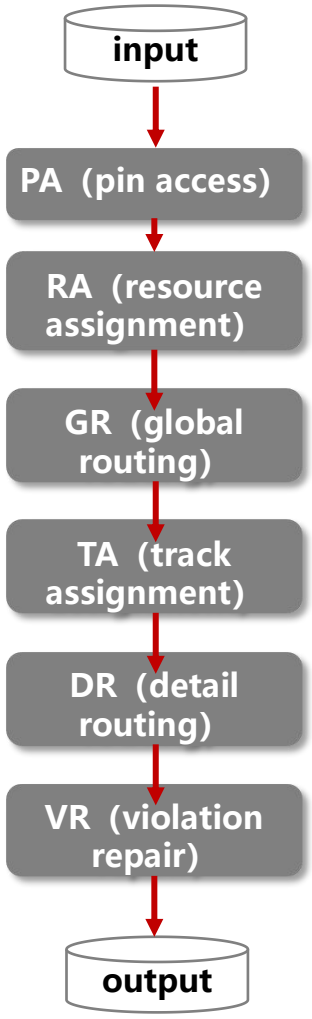


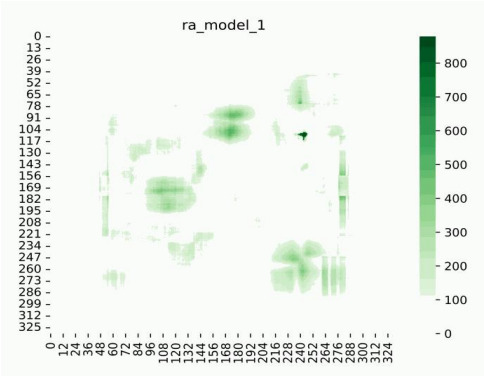
- **Optimization metrics:** wirelength, timing, congestion, DRC
- **Optimization operations:** Global routing: Track allocation: Detailed routing
- **Routing algorithms:** Pattern routing, A* routing, Steiner tree, Non-linear programming, Integer programming

Routing (iRT)

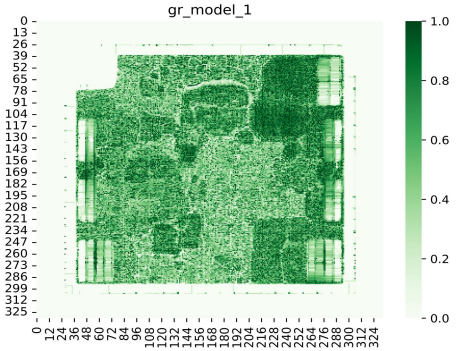
iEDA

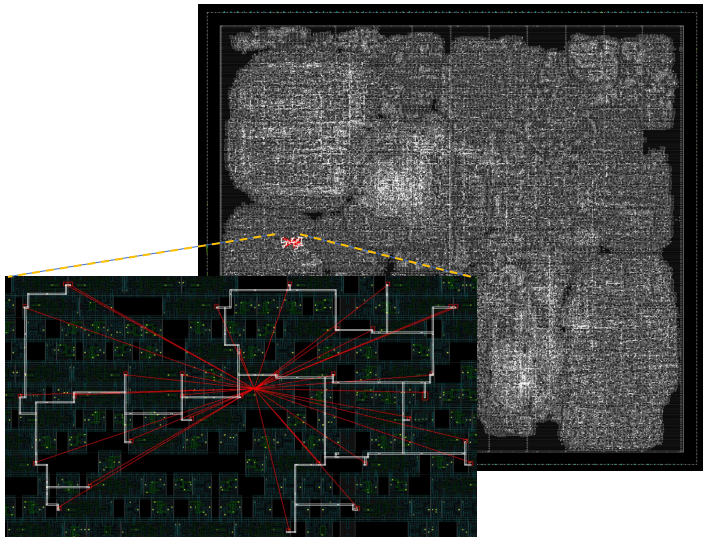
Flow



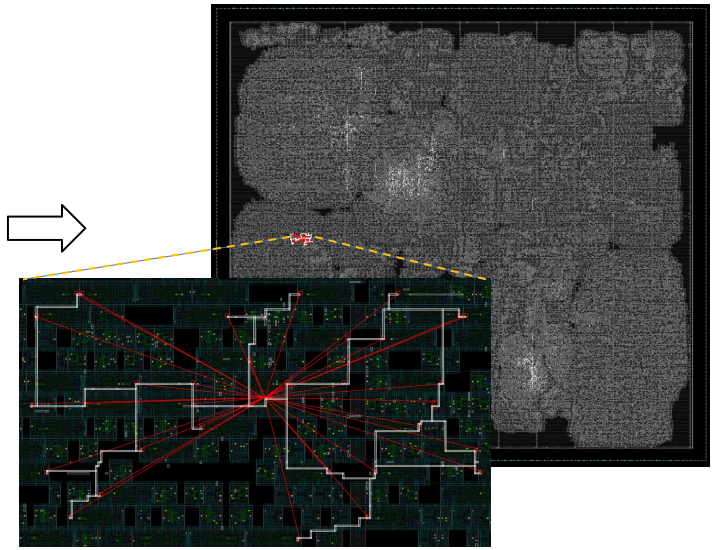


Layout resource/congestion





first iteration routing result



final routing result

Access Type	Pin Number
Track Grid	876856(75.2479%)
On Track	259825(22.297%)
On Shape	28608(2.45501%)
Total	1165289

Routing Layer	Port Number	Access Point Number
M1	806086(68.3279%)	799044(68.5705%)
M2	366214(31.0422%)	362248(31.0865%)
M3	7073(0.599543%)	3997(0.343005%)
M4	358(0.0303459%)	0(0%)
M5	0(0%)	0(0%)
M6	0(0%)	0(0%)
M7	0(0%)	0(0%)
M8	0(0%)	0(0%)
M9	0(0%)	0(0%)
AP	0(0%)	0(0%)
Total	1179731	1165289

Pin Access

Routing Layer	Wire Length / um
M1	9774(0.117785%)
M2	846292(10.1985%)
M3	1.98405e+06(23.9095%)
M4	1.78748e+06(21.5406%)
M5	1.29642e+06(15.6229%)
M6	1.41202e+06(17.016%)
M7	960890(11.5795%)
M8	539.92(0.00650648%)
M9	720(0.00867659%)
AP	0(0%)
Total	8.29819e+06

Cut Layer	Via Number
CO	0(0%)
VIA1	595417(30.6475%)
VIA2	682833(35.147%)
VIA3	400386(20.6088%)
VIA4	135600(6.97965%)
VIA5	89437(4.60353%)
VIA6	38709(1.99244%)
VIA7	262(0.0134857%)
VIA8	148(0.0076179%)
RV	0(0%)
Total	1942792

Resource Overflow	GCell Number
[0,0.1)	921387(83.1%)
[0.1,0.2)	57544(5.19%)
[0.2,0.3)	51492(4.64%)
[0.3,0.4)	40084(3.61%)
[0.4,0.5)	21944(1.98%)
[0.5,0.6)	10780(0.972%)
[0.6,0.7)	4140(0.373%)
[0.7,0.8)	1223(0.11%)
[0.8,0.9)	222(0.02%)
[0.9,1]	74(0.00667%)
Total	1108890

Access Overflow	GCell Number
[0,0.1)	1.78338e+06(80.4%)
[0.1,0.2)	108739(4.9%)
[0.2,0.3)	79939(3.6%)
[0.3,0.4)	90020(4.06%)
[0.4,0.5)	56112(2.53%)
[0.5,0.6)	36741(1.66%)
[0.6,0.7)	30046(1.35%)
[0.7,0.8)	12155(0.548%)
[0.8,0.9)	8771(0.395%)
[0.9,1]	11881(0.536%)
Total	2217780

Wirelength and via

Drc Summary

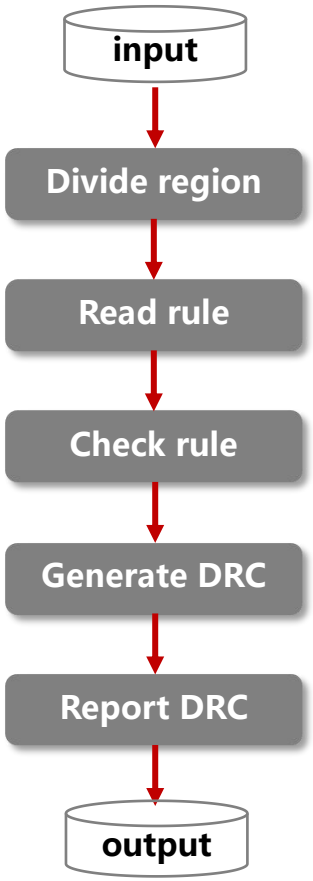
DRC Type	Number
Cut Different Layer Spacing	433141
Cut EOL Spacing	197803
Cut Enclosure	152168
Cut EnclosureEdge	0
Cut Spacing	358281
Metal Corner Filling Spacing	10443
Metal EOL Spacing	869415
Metal JogToJog Spacing	0
Metal Notch Spacing	733497
Metal Parallel Run Length Spacing	864355
Metal Short	1745445
MinHole	1260
MinStep	670823
Minimal Area	1248072

Design rule check

Design Rule Check (iDRC)

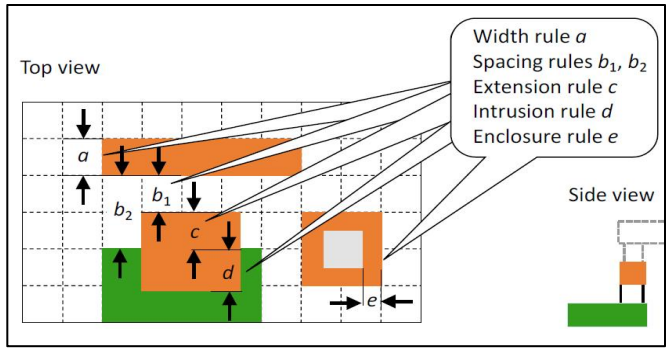
iEDA

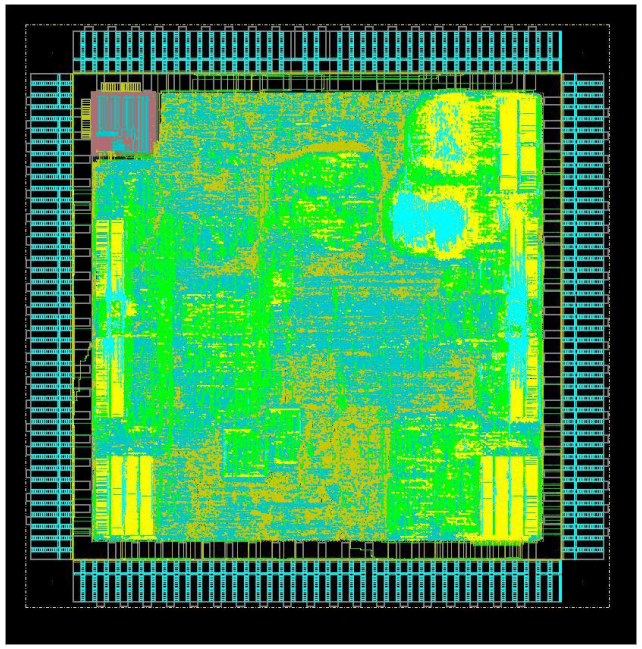
Flow

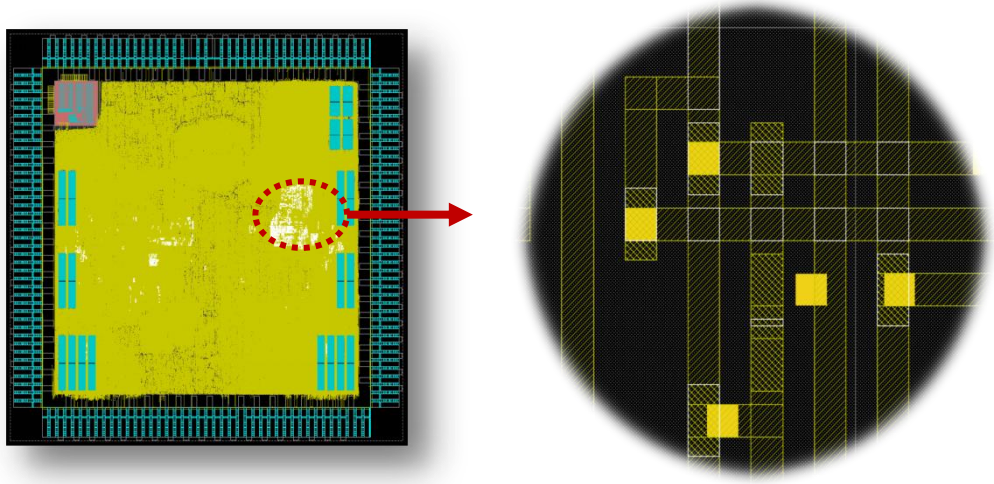


Support DRC Rules:

- Cut Different Layer Spacing
- Cut EOL Spacing
- Cut Enclosure
- Cut Enclosure Edge
- Cut Spacing
- Metal Corner Filling Spacing
- Metal EOL Spacing
- Metal JogToJog Spacing
- Metal Notch Spacing
- Metal Parallel Run Length Spacing
- Metal Short
- MinHole
- MinStep
- Minimal Area





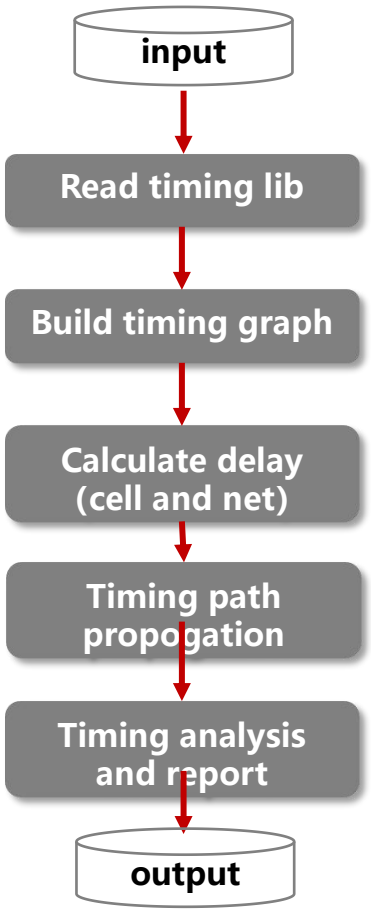


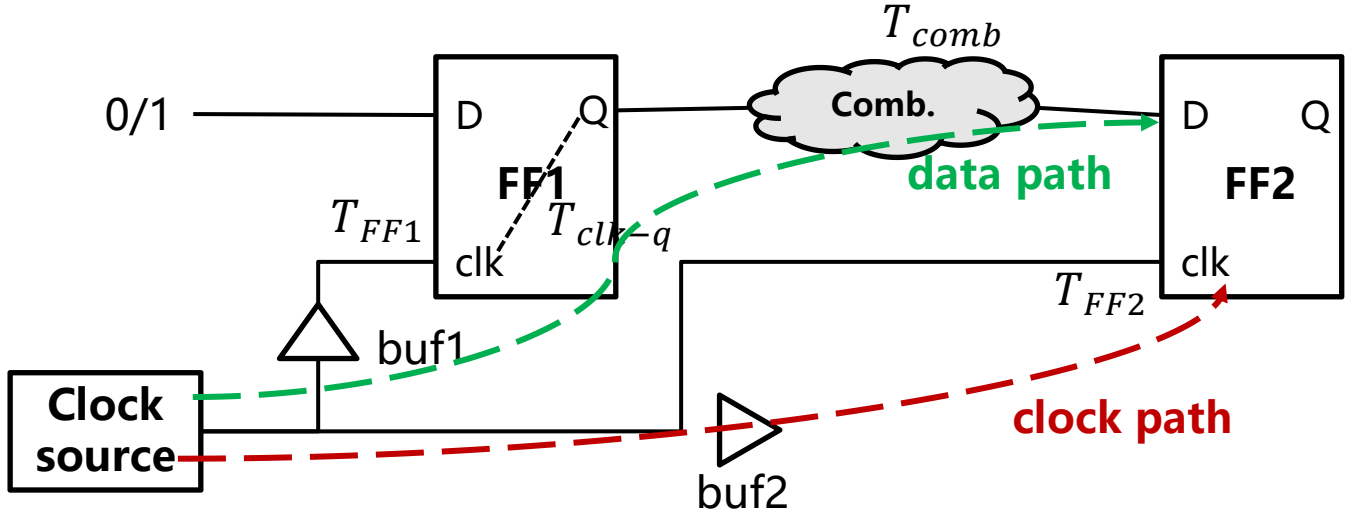
DRC Visulization

Static Timing Analysis (iSTA)

iEDA

FLow





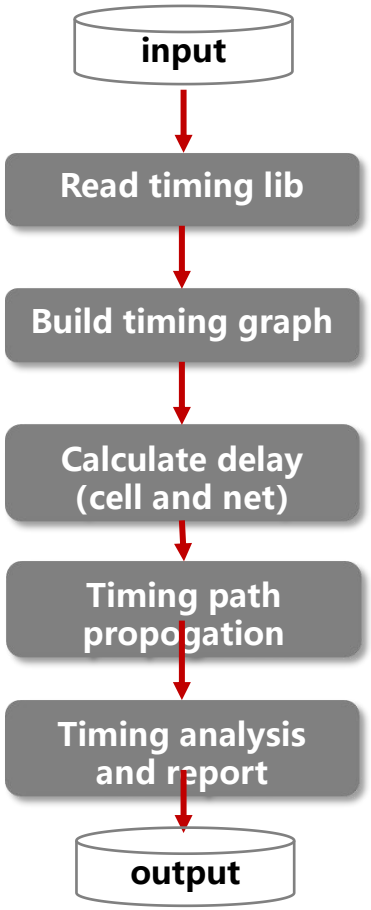
$$T_{FF1} + T_{clk-q} + T_{comb} + T_{setup} - T_{FF2} - T = T^{late}_{slack} \geq 0$$ **Setup Constraint**

$$T_{FF1} + T_{clk-q} + T_{comb} - T_{hold} - T_{FF2} = T^{early}_{slack} \geq 0$$ **Hold Constraint**

Static Timing Analysis (iSTA)

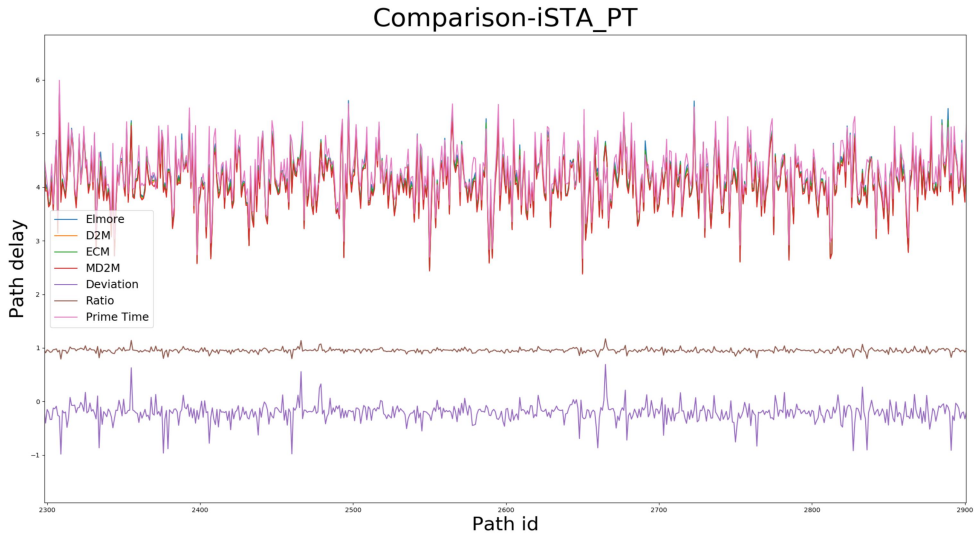
iEDA

FLow



Feature
Support hierarchy netlist and def
Basic setup/hold analysis
Support NLDM/Elmore
Support CCS model
Support high-level net delay model
Support sdf mark
OCV
AOCV
POCV
Consider IRDrop analysis on multi-voltage domain
Hierarchy analysis
Crosstalk analysis
clock gate analysis
Latch analysis

Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		0.885	0.011	0.011r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.011r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		0.885	0.032	0.043r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.043r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		0.885	0.021	0.064r
u0_rcg/mux_core_clk_0 (clock net)	17				0.000			
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.064	0.064
u0_rcg/mux_core_clk_div3/gt_en1_reg:CP (DFSNQD1BWP40P140LVT)		0.000	0.000	0.015		1.000	0.000	0.064r
u0_rcg/mux_core_clk_div3/gt_en1_reg:Q (DFSNQD1BWP40P140LVT)		0.001	0.000	0.009		0.820	0.045	0.109r
u0_rcg/mux_core_clk_div3/gt_en1 (net)	1				0.000			
u0_rcg/mux_core_clk_div3/U_GT1:E (CKLNQD4BWP40P140LVT)		0.001	0.000	0.009		1.000	0.000	0.109r
u1_clk:XC (PDXOEDG_V_G)		0.002	0.000	0.000		1.000	0.000	0.000r
sys_clk_100m (clock net)	1				0.000			
u1_clk_xc_donottouch:I (CKBD12BWP40P140LVT)		0.002	0.000	0.000		1.000	0.000	0.000r
u1_clk_xc_donottouch:Z (CKBD12BWP40P140LVT)		0.002	0.000	0.006		1.039	0.013	0.013r
sys_clk_100m_buf (clock net)	2				0.000			
u0_rcg/u1_lvt_ckmux2hdv4:I0 (CKMUX2D4BWP40P140LVT)		0.001	0.000	0.006		1.000	0.000	0.013r
u0_rcg/u1_lvt_ckmux2hdv4:Z (CKMUX2D4BWP40P140LVT)		0.006	0.000	0.018		1.039	0.038	0.051r
u0_rcg/mux_core_clk (clock net)	5				0.000			
u0_rcg/mux_core_clk_0_buf:I (CKBD4BWP35P140)		0.001	0.000	0.018		1.000	0.000	0.051r
u0_rcg/mux_core_clk_0_buf:Z (CKBD4BWP35P140)		0.008	0.000	0.015		1.039	0.025	0.076r
u0_rcg/mux_core_clk_0 (clock net)	17				NA			
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)		0.001	0.000	0.000		1.000	0.000	0.076r
clock CLK_u1_clk_XC (rise edge)							0	0
clock network delay (propagated)							0.076	0.076
u0_rcg/mux_core_clk_div3/U_GT1:CP (CKLNQD4BWP40P140LVT)								r
library hold time							0.000	0.076
clock reconvergence pessimism						-0.011	0.064	
data require time								0.064
data arrival time								0.109
slack (MET)								0.045

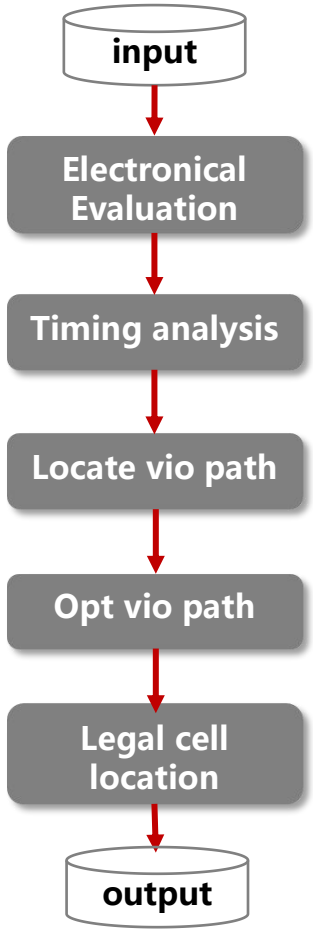


pt/ista ratio	value
mean	1.11
variance	0.00095
median	1.107
maximum	1.5404
minimum	0.9035

Timing Optimization (iTO)

iEDA

Flow



Key parameter config	
Input	iPL.def, iCTS.def
output	iTO_setup_result.def, iTO_hold_reslut.def
setup_slack_margin	setup slack value
hold_slack_margin	hold slack value
max_buffer_percent	Area ratio of inserted buffer
max_utilization	Core utilization
DRV_insert_buffers	Available buffer for optimizing DRV
setup_insert_buffers	Available buffer for optimizing setup
hold_insert_buffers	Available buffer for optimizing hold
number_passes_allowed_decreasing_slack	The number of times that WNS is allowed continuously decrease when opt setup
rebuffer_max_fanout	For setup, a wire network is not optimized for buffer insertion when its fanout exceeds this value
split_load_min_fanout	For setup, fanout is reduced by inserting a buffer when fanout is greater than this value

DRV report

```
path
Worst Slack: -5.88383
Found 3 slew violations.
Found 11 capacitance violations.
Found 0 fanout violations.
Found 0 long wires.
Before ViolationFix | slew_vio: 3 cap_vio: 11 fanout_vio: 0 length_vio: 0
The 1th check
After ViolationFix | slew_vio: 3 cap_vio: 0 fanout_vio: 0 length_vio: 0
The 2th check
After ViolationFix | slew_vio: 0 cap_vio: 0 fanout_vio: 0 length_vio: 0
DRV_net_3
Inserted 11 buffers in 12 nets.
Resized 0 instances.
```

Setup report

```
Inserted 10 hold buffers.

Worst Hold Path Launch : u0_soc_top/u0_sdram_axi/u_core/sample_data0_q_reg_8_:CP
Worst Hold Path Capture: u0_soc_top/u0_sdram_axi/u_core/sample_data_q_reg_8_:CP

The 1-th timing check.
    worst hold slack: -1.28225
Unable to repair all hold violations. There are still 16 endpoints with hold violation.
Max utilization reached.
```

- Fix timing design rule violation
  - Max cap/Max slew/Max wirelength/Max fanout
- Fix hold time
- Fix setup time
- Cell sizing
- Buffer Insertion
- Load Insertion
- Buffer/load location

Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	-185.768	-1.27825
CLK_div2_core	-2606.7	-0.106129
CLK_div2_hs_peri	-216.759	-0.028571
CLK_div3_hs_peri	-72.5124	-0.028571
CLK_div4_core	-1304.1	-0.106129
CLK_div4_hs_peri	-185.768	-1.27825
CLK_div4_peri	-231.408	-0.042802
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	-89.8732	-0.028408
CLK_u0_clk_XC	-2987.42	-0.106129
CLK_u0_pll_FOUTPOSTDIV	-8546.64	-0.106129
CLK_u1_clk_XC	-2755.16	-0.106129

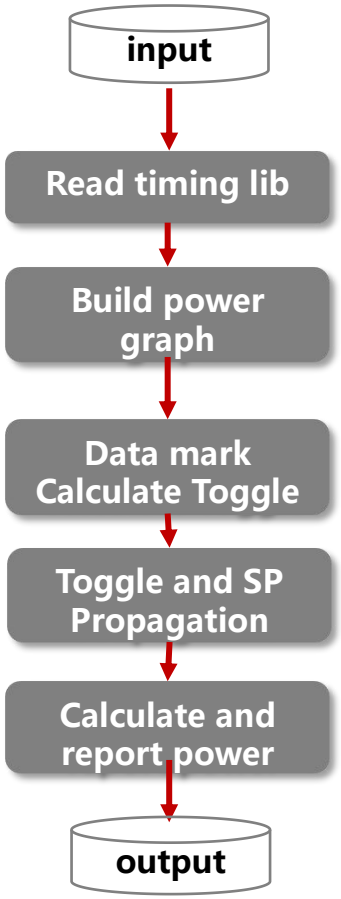
Clock Group	Hold TNS	Hold WNS
CLK_chiplink_tx_clk	0	0
CLK_clk_hs_peri	0	0
CLK_div2_core	0	0
CLK_div2_hs_peri	0	0
CLK_div3_hs_peri	0	0
CLK_div4_core	0	0
CLK_div4_hs_peri	0	0
CLK_div4_peri	0	0
CLK_sdram_clk_o	0	0
CLK_spi_clk	0	0
CLK_spi_clk_out	0	0
CLK_u0_chiplink_rx_clk_pad_PAD	0	0
CLK_u0_clk_XC	0	0
CLK_u0_pll_FOUTPOSTDIV	0	0
CLK_u1_clk_XC	0	0

Hold report

Power Analysis (iPA)

iEDA

Flow



API	Description
buildGraph	Build iPW graph data structure
readVCD	Parse the VCD file
buildSeqGraph	Build timing subgraph
checkPipelineLoop	Detect PipeLine loop
levelizeSeqGraph	Grade timing subgraph
propagateToggleSP	Propagate Toggle and SP data on the graph
calcLeakagePower	Calculate the leakage power
calcInternalPower	Calculate internal power
calcSwitchPower	Calculate switching power
analyzeGroupPower	Analyze power data
reportPower	Output power report

cases	iPA total power	Innovus total power	deviation
aes_cipher_top	22.22mW	23.74mW	6.4%
gcd	0.38mW	0.37mW	3.6%
uart	0.51mW	0.49mW	3.9%

```
Generate the report at 2023-05-06T09:54:06
Report : Averaged Power
+--------------+----------------+--------------+--------------+-------------+-----------+
| Power Group  | Internal Power | Switch Power | Leakage Power | Total Power | (%)       |
+--------------+----------------+--------------+--------------+-------------+-----------+
| combinational | 1.064e-07     | 5.063e-09    | 3.079e-08    | 1.422e-07   | (27.595%) |
| sequential   | 2.862e-07      | 7.337e-09    | 7.963e-08    | 3.732e-07   | (72.405%) |
+--------------+----------------+--------------+--------------+-------------+-----------+
Net Switch Power   ==   1.240e-08 (2.406%)
Cell Internal Power   ==   3.926e-07 (76.173%)
Cell Leakage Power   ==   1.104e-07 (21.422%)
Total Power   ==   5.154e-07
```

- Evaluate power before / during / after the physical design process
- Average model
- Timing window (coming soon)
- VCD parser
- Report/API

iEDA

01 Introduction

02 iEDA

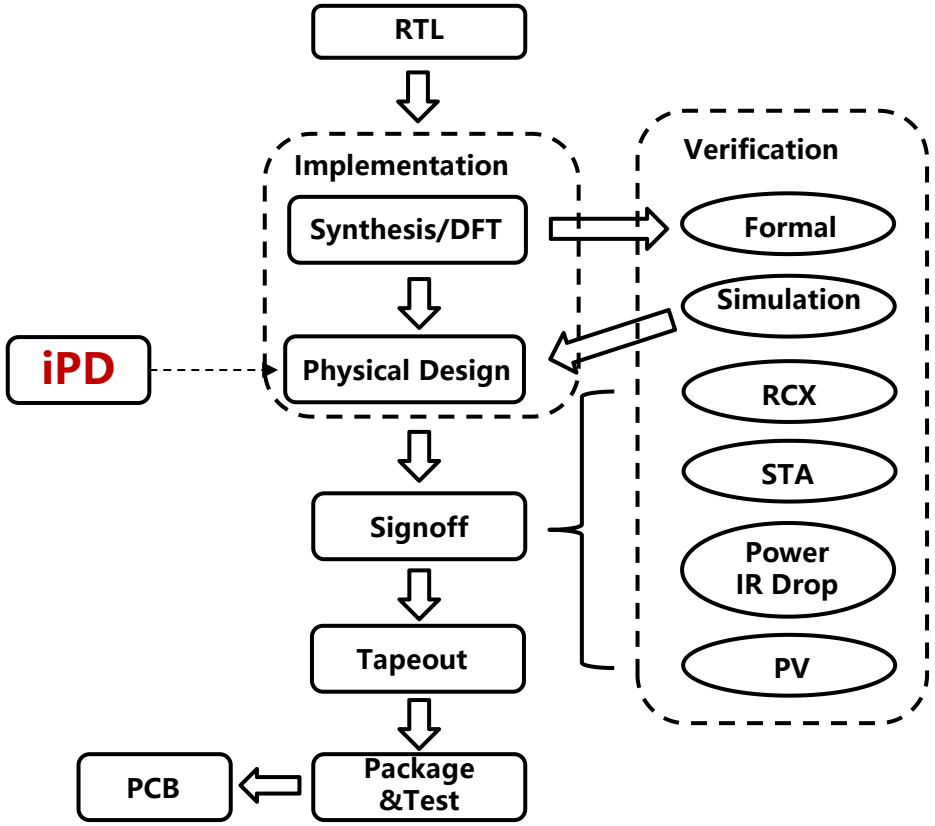
03 iEDA Design Chip

04 iEDA Community

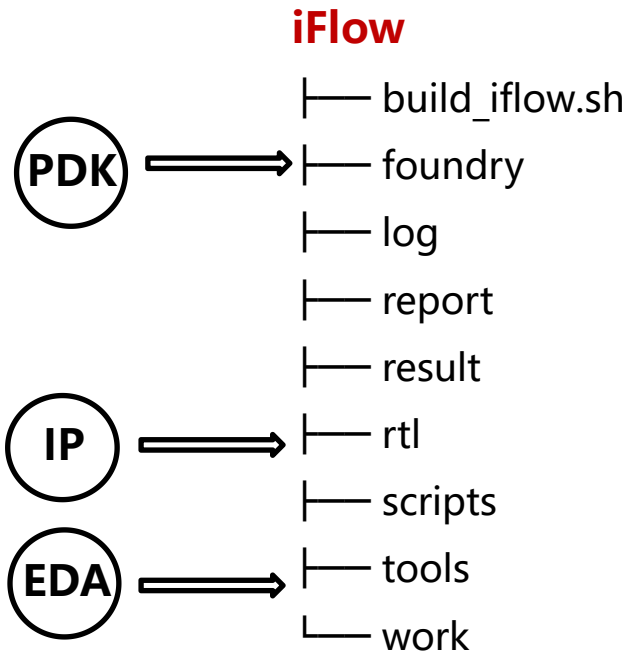
iFlow: A Chip Design Flow

iEDA

- **iFlow: supporting different EDA tools, PDKs, designs**



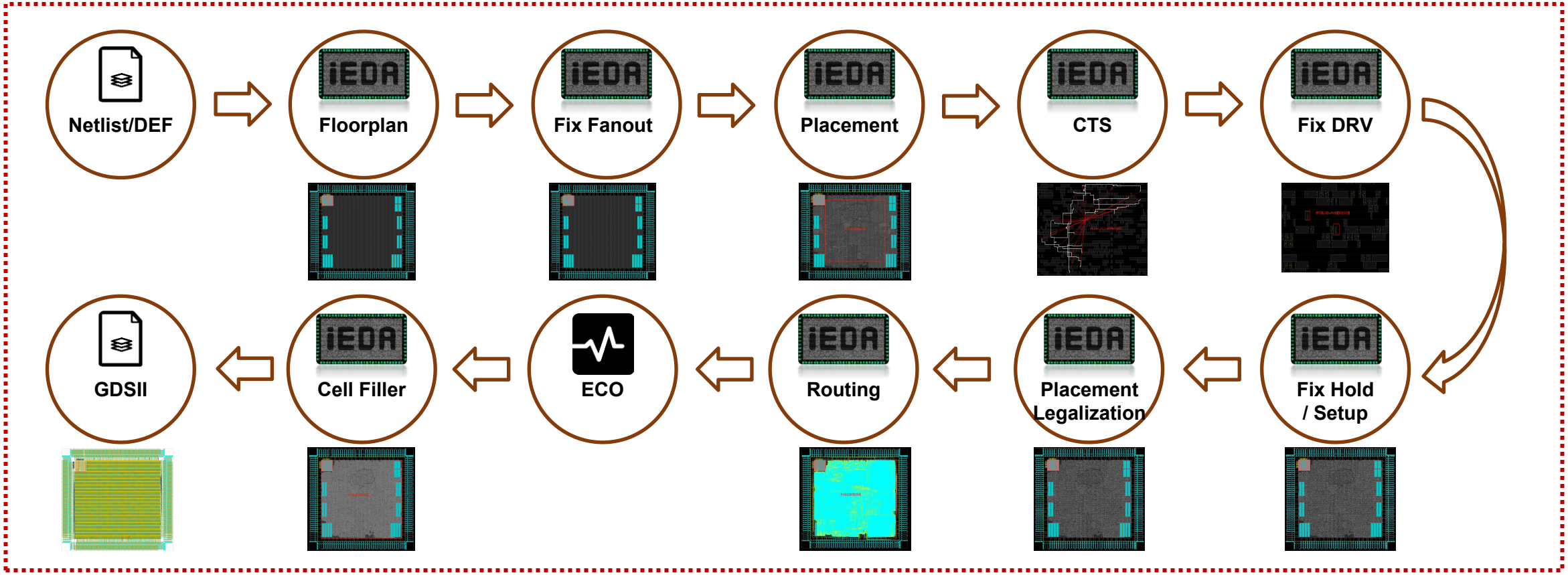
Chip design flow



Flow: Netlist -> GDSII

iEDA

- ✓ Enabling the Physical Design Flow,
- ✓ Supporting Technologies: 110nm, 28nm, Open-source Technologies (Sky130, Nangate45)



iEDA Physical Design Flow

Environment Config

iEDA

- **Userguide:** https://gitee.com/oscc-project/iEDA/blob/master/docs/user_guide/iEDA_user_guide.md

Download and Compile iEDA

```
# 下载iEDA仓库
git clone https://gitee.com/oscc-project/iEDA.git iEDA && cd iEDA
# 通过apt安装编译依赖，需要root权限
sudo bash build.sh -i apt
# 编译 iEDA
bash build.sh -j 16
# 若能够正常输出 "Hello iEDA!" 则编译成功
./bin/iEDA -script scripts/hello.tcl
```

拷贝 ./bin/iEDA 到目录 ./scripts/design/sky130_gcd

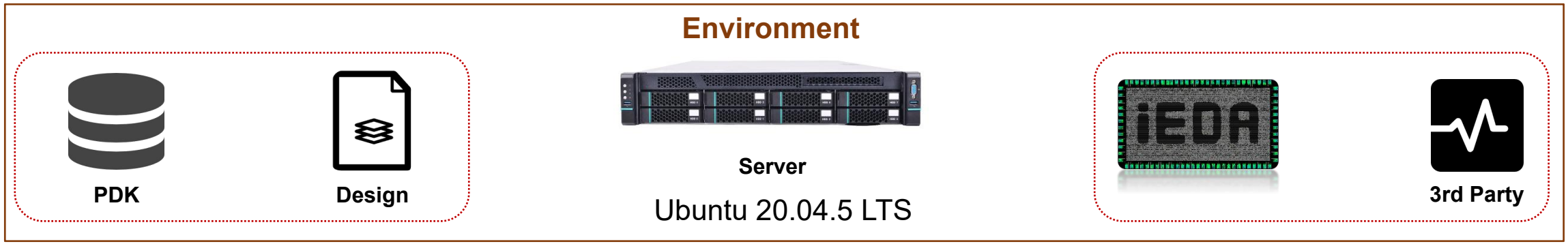
```
# 拷贝 iEDA 到sky130 目录
cp ./bin/iEDA scripts/design/sky130_gcd/.
```

Design

- ✓ Netlist

(28nm) Library

- ✓ TechLEF
- ✓ Std Cell LEF
- ✓ liberty
- ✓ sdc
- ✓ (spef)



TCL Script

```
├── design                    #iEDA flows for different designs
│   ├── ispd18                #tbd
│   └── sky130_gcd            #flow of gcd in sky130
│       ├── iEDA
│       ├── iEDA_config       # iEDA parameters configuration files
│       ├── README.md
│       ├── result            # iEDA result output files
│       ├── run_iEDA_gui.py   # Python3 script for running all iEDA flow with GUI layout
│       ├── run_iEDA.py       # Python3 script for running all iEDA flow
│       ├── run_iEDA.sh       # POSIX shell script for running all iEDA flow
│       └── script            # TCL script files
├── foundry
│   ├── README.md
│   └── sky130                # SkyWater Open Source PDK
│       ├── lef               # lef files
│       ├── lib               # lib files
│       ├── sdc               # sdc files
│       └── spef              # folder for spef files if needed
└── hello.tcl                 # Test running iEDA
```

```
├── DB_script                          # Data process flow scripts
│   ├── db_init_lef.tcl                # initialize lef
│   ├── db_init_lib_drv.tcl            # initialize lib only for flow of drv
│   ├── db_init_lib_fixfanout.tcl      # initialize lib only for flow of fix fanout
│   ├── db_init_lib_hold.tcl           # initialize lib only for flow of optimize hold
│   ├── db_init_lib_setup.tcl          # initialize lib only for flow of optimize setup
│   ├── db_init_lib.tcl                # initialize lib for common flow
│   ├── db_init_sdc.tcl                # initialize sdc
│   ├── db_init_spef.tcl               # initialize spef
│   ├── db_path_setting.tcl            # set paths for all processing technology files, including TechLEF. LEF, Lib, sdc and sp
│   ├── run_db_checknet.tcl            # check net connectivity based on data built by DEF (.def) and LEF (.lef & .tlef)
│   ├── run_db_report_evl.tcl          # report wire length and congestion based on data built by DEF (.def) and LEF (.lef & .
│   ├── run_db.tcl                     # test building data by DEF (.def) and LEF (.lef & .tlef)
│   ├── run_def_to_gds_text.tcl        # transform data from DEF (.def) to GDSII (.gdsii)
│   ├── run_def_to_verilog.tcl         # transform data from DEF (.def) to netlist (.v)
│   ├── run_netlist_to_def.tcl         # transform data from netlist (.v) to DEF (.def)
│   └── run_read_verilog.tcl           # test read verilog file (.v)
├── iCTS_script                        # CTS flow scripts
│   ├── run_iCTS_eval.tcl              # report wire legnth for CTS result
│   ├── run_iCTS_STA.tcl               # report CTS STA
│   └── run_iCTS.tcl                   # run CTS
├── iDRC_script                        # DRC(Design Rule Check) flow scipts
│   ├── run_iDRC_gui.tcl               # show GUI for DRC result
│   └── run_iDRC.tcl                   # run DRC
├── iFP_script                         # Floorplan flow scripts
│   ├── module                         # submodule for Floorplan scripts
│   │   ├── create_tracks.tcl          # create tracks for routing layers
│   │   ├── pdn.tcl                    # create pdn networks
│   │   └── set_clocknet.tcl           # set clock net
│   └── run_iFP.tcl                    # run Floorplan
├── iGUI_script                        # GUI flow scipts
│   └── run_iGUI.tcl                   # run GUI
├── iNO_script                         # NO(Netlist Optimization) flow scipts
│   └── run_iNO_fix_fanout.tcl         # run Fix Fanout
├── iPL_script                         # Placement flow scripts
│   ├── run_iPL_eval.tcl               # report congestion statistics and wire legnth for Placement result
│   ├── run_iPL_filler.tcl             # run standard cell filler
```

TCL Script

iEDA

Flow

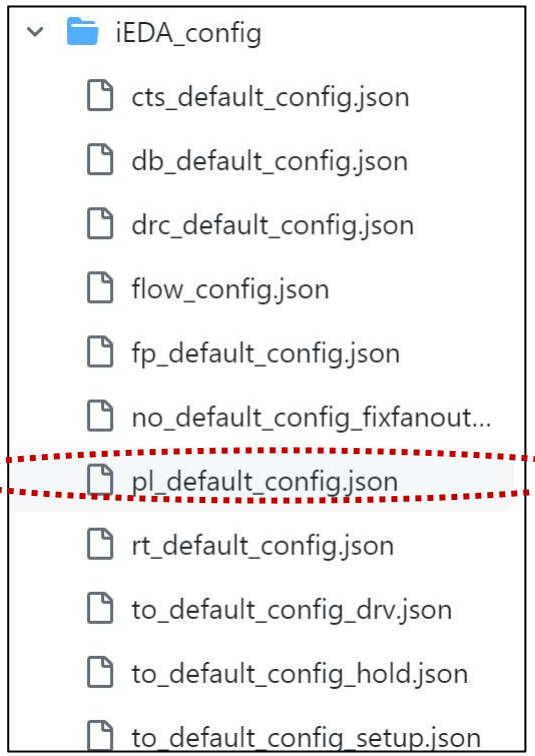
```
#============================================================
##   run floorplan
#============================================================
os.system('./iEDA -script ./script/iFP_script/run_iFP.tcl')
#============================================================
##   run NO -- fix fanout
#============================================================
os.system('./iEDA -script ./script/iNO_script/run_iNO_fix_fanout.tcl')
#============================================================
##   run Placer
#============================================================
os.system('./iEDA -script ./script/iPL_script/run_iPL.tcl')
os.system('./iEDA -script ./script/iPL_script/run_iPL_eval.tcl')
# ============================================================
#   run CTS
# ============================================================
os.system('./iEDA -script ./script/iCTS_script/run_iCTS.tcl')
os.system('./iEDA -script ./script/iCTS_script/run_iCTS_eval.tcl')
os.system('./iEDA -script ./script/iCTS_script/run_iCTS_STA.tcl')
#============================================================
##   run TO -- fix_drv
#============================================================
os.system('./iEDA -script ./script/iTO_script/run_iTO_drv.tcl')
os.system('./iEDA -script ./script/iTO_script/run_iTO_drv_STA.tcl')
#============================================================
#   run TO -- opt_hold
#============================================================
os.system('./iEDA -script ./script/iTO_script/run_iTO_setup.tcl')
os.system('./iEDA -script ./script/iTO_script/run_iTO_hold.tcl')
os.system('./iEDA -script ./script/iTO_script/run_iTO_hold_STA.tcl')
#============================================================
#   run PL Incremental Flow
#============================================================
os.system('./iEDA -script ./script/iPL_script/run_iPL_legalization.tcl')
os.system('./iEDA -script ./script/iPL_script/run_iPL_legalization_eval.tcl')
# ============================================================
# #   run Router
# ============================================================
os.system('./iEDA -script ./script/iRT_script/run_iRT.tcl')
os.system('./iEDA -script ./script/iRT_script/run_iRT_eval.tcl')
os.system('./iEDA -script ./script/iRT_script/run_iRT_STA.tcl')
os.system('./iEDA -script ./script/iRT_script/run_iRT_DRC.tcl')
#============================================================
##   run Filler
#============================================================
os.system('./iEDA -script ./script/iPL_script/run_iPL_filler.tcl')
#============================================================
##   run def to gdsii
#============================================================
os.system('./iEDA -script ./script/DB_script/run_def_to_gds_text.tcl')
```

Placement

```
#============================================================
##   init flow config
#============================================================
flow_init -config ./iEDA_config/flow_config.json
#============================================================
##   read db config
#============================================================
db_init -config ./iEDA_config/db_default_config.json
#============================================================
##   reset data path
#============================================================
source ./script/DB_script/db_path_setting.tcl
#============================================================
##   reset sdc
#============================================================
source ./script/DB_script/db_init_sdc.tcl
#============================================================
##   read lef
#============================================================
source ./script/DB_script/db_init_lef.tcl
#============================================================
##   read def
#============================================================
def_init -path ./result/iTO_fix_fanout_result.def
#============================================================
##   run Placer
#============================================================
run_placer -config ./iEDA_config/pl_default_config.json
#============================================================
##   Save def
#============================================================
def_save -path ./result/iPL_result.def
#============================================================
##   Save netlist
#============================================================
netlist_save -path ./result/iPL_result.v -exclude_cell_names {}
#============================================================
##   report
#============================================================
report_db -path "./result/report/pl_db.rpt"
#============================================================
##   Exit
#============================================================
flow_exit
```

Parameter Config

- Config



iEDA / scripts / design / sky130_gcd / iEDA_config / pl_default_config.json

Code | Blame | 82 lines (82 loc) · 2.38 KB

```
3           "is_max_length_opt": 0,
4           "max_length_constraint": 1000000,
5           "is_timing_effort": 0,
6           "is_congestion_effort": 0,
7           "ignore_net_degree": 100,
8           "num_threads": 1,
9           "GP": {
10              "Wirelength": {
11                  "init_wirelength_coef": 0.25,
12                  "reference_hpwl": 446000000,
13                  "min_wirelength_force_bar": -300
14              },
15              "Density": {
16                  "target_density": 0.8,
17                  "bin_cnt_x": 128,
18                  "bin_cnt_y": 128
19              },
20              "Nesterov": {
21                  "max_iter": 2000,
22                  "max_backtrack": 10,
23                  "init_density_penalty": 0.00008,
24                  "target_overflow": 0.1,
25                  "initial_prev_coordi_update_coef": 100,
26                  "min_precondition": 1.0,
27                  "min_phi_coef": 0.95,
28                  "max_phi_coef": 1.05
29              }
30          },
31          "BUFFER": {
32              "max_buffer_num": 10000,
33              "buffer_type": [
34                  "sky130_fd_sc_hs__buf_1"
35              ]
36          },
37          "LG": {
38              "max_displacement": 1000000,
39              "global_right_padding": 0
```

iEDA / scripts / design / sky130_gcd / iEDA_config / pl_default_config.json

Code | Blame | 82 lines (82 loc) · 2.38 KB

```
42              "max_displacement": 1000000,
43              "global_right_padding": 0,
44              "enable_networkflow" : 0
45          },
46          "Filler": {
47              "first_iter": [
48                  "sky130_fd_sc_hs__fill_8",
49                  "sky130_fd_sc_hs__fill_4",
50                  "sky130_fd_sc_hs__fill_2",
51                  "sky130_fd_sc_hs__fill_1"
52              ],
53              "second_iter": [
54                  "sky130_fd_sc_hs__fill_8",
55                  "sky130_fd_sc_hs__fill_4",
56                  "sky130_fd_sc_hs__fill_2",
57                  "sky130_fd_sc_hs__fill_1"
58              ],
59              "min_filler_width": 1
60          },
61          "MP": {
62              "fixed_macro": [],
63              "fixed_macro_coordinate": [],
64              "blockage": [],
65              "guidance_macro": [],
66              "guidance": [],
67              "solution_type": "BStarTree",
68              "SimulateAnneal": {
69                  "perturb_per_step": 100,
70                  "cool_rate": 0.92
71              },
72              "Partition": {
73                  "parts": 66,
74                  "ufactor": 100,
75                  "new_macro_density": 0.6
76              },
77              "halo_x": 0,
78              "halo_y": 0,
79              "output_path": "${RESULT_DIR}/pl/"
```

How to Run Netlist -> GDSII Flow by iEDA

Flow	Script	Config	Design Input
布图规划 (Floorpan)	./iEDA -script ./script/iFP_script/run_iFP.tcl		./result/verilog/gcd.v
网表优化（Fix Fanout）	./iEDA -script ./script/iNO_script/run_iNO_fix_fanout.tcl	./iEDA_config/cts_default_config.json	./result/iFP_result.def
布局 (Placement)	./iEDA -script ./script/iPL_script/run_iPL.tcl	./iEDA_config/pl_default_config.json	./result/iTO_fix_fanout_resu
布局结果评估 (评估线长和拥塞)	./iEDA -script ./script/iPL_script/run_iPL_eval.tcl		./result/iPL_result.def
时钟树综合 (CTS)	./iEDA -script ./script/iCTS_script/run_iCTS.tcl	./iEDA_config/cts_default_config.json	./result/iPL_result.def
时钟树综合结果评估 (评估线长)	./iEDA -script ./script/iCTS_script/run_iCTS_eval.tcl		./result/iCTS_result.def
时钟树综合时序评估 (评估时序)	./iEDA -script ./script/iCTS_script/run_iCTS_STA.tcl		./result/iCTS_result.def
修复DRV违例 (Fix DRV Violation)	./iEDA -script ./script/iTO_script/run_iTO_drv.tcl	./iEDA_config/to_default_config_drv.json	./result/iCTS_result.def
Fix DRV结果评估 (评估时序)	./iEDA -script ./script/iTO_script/run_iTO_drv_STA.tcl		./result/iTO_drv_result.def
修复Hold违例（Fix Hold Violation）	./iEDA -script ./script/iTO_script/run_iTO_hold.tcl	./iEDA_config/to_default_config_hold.json	./result/iTO_drv_result.def
Fix Hold结果评估（评估时序）	./iEDA -script ./script/iTO_script/run_iTO_hold_STA.tcl		./result/iTO_hold_result.def
单元合法化（Legalization）	./iEDA -script ./script/iPL_script/run_iPL_legalization.tcl	./iEDA_config/pl_default_config.json	./result/iTO_hold_result.def
合法化结果评估（评估线长和拥塞）	./iEDA -script ./script/iPL_script/run_iPL_legalization_eval.tcl		./result/iPL_lg_result.def
布线（Routing）	./iEDA -script ./script/iRT_script/run_iRT.tcl		./result/iPL_lg_result.def

Report

✓ Statistics

- iFP
- iNO
- iPL
- iCTS
- iTO
- iRT

```
#################################################################
Summary
+-----------------------+-----------------------------------------+
| Module                | Value                                   |
+-----------------------+-----------------------------------------+
| DIE Area ( um^2 )     | 2249940.000000 = 1499.960000 * 1500.000000 |
| DIE Usage             | 0.237865                                |
| CORE Area ( um^2 )    | 1340542.224000 = 1160.040000 * 1155.600000 |
| CORE Usage            | 0.399228                                |
|                       |                                         |
| Number - Site         | 9                                       |
| Number - Row          | 1284                                    |
| Number - Track        | 20                                      |
| Number - Layer        | 32                                      |
| Number - Routing Layer | 10                                     |
| Number - Cut Layer    | 10                                      |
| Number - GCell Grid   | 5                                       |
| Number - Cell Master  | 16314                                   |
| Number - Via Rule     | 492                                     |
|                       |                                         |
| Number - IO Pin       | 110                                     |
| Number - Instance     | 362883                                  |
| Number - Blockage     | 21                                      |
| Number - Filler       | 0                                       |
| Number - Net          | 377248                                  |
| Number - Special Net  | 5                                       |
+-----------------------+-----------------------------------------+
```

✓ Design rule violations

- iRT

```
Drc Summary
+-----------------------------------+---------+
| DRC Type                          | Number  |
+-----------------------------------+---------+
| Cut Different Layer Spacing       | 0       |
| Cut EOL Spacing                   | 0       |
| Cut Enclosure                     | 610489  |
| Cut EnclosureEdge                 | 0       |
| Cut Spacing                       | 264504  |
| Metal Corner Filling Spacing      | 0       |
| Metal EOL Spacing                 | 8404599 |
| Metal JogToJog Spacing            | 0       |
| Metal Notch Spacing               | 1621088 |
| Metal Parallel Run Length Spacing | 3253512 |
| Metal Short                       | 6429817 |
| MinHole                           | 94      |
| MinStep                           | 7794204 |
| Minimal Area                      | 744067  |
+-----------------------------------+---------+
```

✓ Evaluation

- Placement
- CTS
- Physical Incremental
- Routing

```
Congestion Report
+-------------------------+---------------+-------------+
| Grid Bin Size           | Bin Partition | Total Count |
+-------------------------+---------------+-------------+
| 9063 * 9029             | 256 by 256    | 65536       |
+-------------------------+---------------+-------------+
| Instance Density Range  | Bins Count    | Percentage  |
+-------------------------+---------------+-------------+
| 0.95 ~ 1.00             | 5372          | 8.20        |
| 0.90 ~ 0.95             | 34            | 0.05        |
| 0.85 ~ 0.90             | 29            | 0.04        |
| 0.80 ~ 0.85             | 329           | 0.50        |
| 0.75 ~ 0.80             | 0             | 0.00        |
+-------------------------+---------------+-------------+
| Pin Count Range         | Bins Count    | Percentage  |
+-------------------------+---------------+-------------+
| 205 ~ 228               | 22            | 0.03        |
| 182 ~ 205               | 129           | 0.20        |
| 160 ~ 182               | 514           | 0.78        |
| 137 ~ 160               | 1555          | 2.37        |
| 114 ~ 137               | 252           | 0.38        |
+-------------------------+---------------+-------------+
```

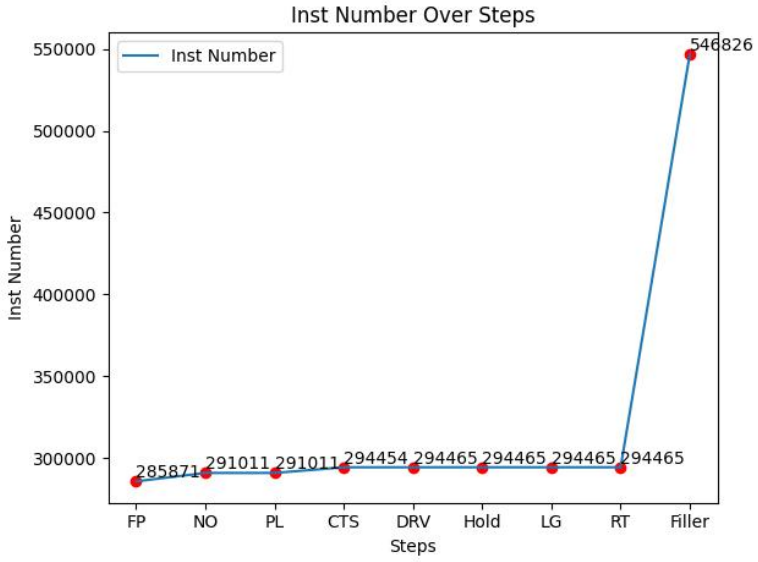
✓ Timing & Power

- Setup, Hold, Violations, Power
- Placement, CTS，Fix DRV，Fix Setup/Hold，Routing

Point	Fanout	Capacitance	Resistance	Transition	Delta Delay	Derate	Incr	Path
spi_miso_pad (port)		8.0000000	0.0010000	0.0000000		1.0000000	0.0000000	0.0000000r
clock CLK_spi_clk_out (rise edge)							0	0
clock network delay (propagated)							0.0000000	0.0000000
spi_miso_pad (port)		8.0000000	0.0010000	0.0000000		1.0000000	29.1000000	29.1000000r
spi_miso_pad (net)	2				0.0000000			
u0_spi_miso:PAD (PDDW04DGZ_H_G)		1.0906020	0.0000000	0.0000000		1.0000000	0.0000000	29.1000000r
u0_spi_miso:C (PDDW04DGZ_H_G)		0.0250522	0.0000000	0.0172830		1.0765001	0.8057400	29.9057400r
spi_flash_miso (net)	1				0.0000000			
ediFE_PDC3389_spi_flash_miso:I (BUFFD16BWP35P140LVT)		0.0028179	2612.1424828	0.0172830		1.0000000	0.0000000	29.9057400r
ediFE_PDC3389_spi_flash_miso:Z (BUFFD16BWP35P140LVT)		0.0197853	0.0000000	0.0106300		1.0765001	0.0217290	29.9274690r
FE_PDN3389_spi_flash_miso (net)	1				0.0000000			
ediFE_PDC12025_spi_flash_miso:I (BUFFD4BWP30P140LVT)		0.0011448	1760.8977135	0.0106300		1.0000000	0.0000000	29.9274690r
ediFE_PDC12025_spi_flash_miso:Z (BUFFD4BWP30P140LVT)		0.0236758	0.0000000	0.0271790		1.0765001	0.0263400	29.9538090r
FE_PDN12025_spi_flash_miso (net)	1				0.0000000			
u0_soc_top/u0_spi_flash/u0_spi_top/shift/U358:A1 (INR2D1BWP40P140LVT)		0.0005121	1727.8863792	0.0194320		1.0000000	0.0129420	29.9667510r
u0_soc_top/u0_spi_flash/u0_spi_top/shift/U358:ZN (INR2D1BWP40P140LVT)		0.0012539	0.0000000	0.0186460		1.0765001	0.0294440	29.9961950r
u0_soc_top/u0_spi_flash/u0_spi_top/shift/n787 (clock net)	1				0.0000000			
ediFE_PDC6804_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:I (BUFFD3BWP30P140LVT)		0.0005980	92.1830030	0.0057640		1.0000000	0.0000140	29.9962090r
ediFE_PDC6804_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:Z (BUFFD3BWP30P140LVT)		0.0329341	0.0000000	0.0510340		1.0765001	0.0428270	30.0390360r
FE_PDN6804_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787 (clock net)	29				0.0000000			
ediFE_PDC6803_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:I (BUFFD3BWP30P140LVT)		0.0005980	701.9384875	0.0107370		1.0000000	0.0085510	30.0475870r
ediFE_PDC6803_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:Z (BUFFD3BWP30P140LVT)		0.0327282	0.0000000	0.0507560		1.0765001	0.0440820	30.0916690r
FE_PDN6803_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787 (clock net)	24				0.0000000			
ediFE_PDC6802_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:I (BUFFD2BWP35P140LVT)		0.0006282	900.9526939	0.0136380		1.0000000	0.0107520	30.1024210r
ediFE_PDC6802_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:Z (BUFFD2BWP35P140LVT)		0.0117069	0.0000000	0.0301890		1.0765001	0.0326970	30.1351180r
FE_PDN6802_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787 (clock net)	10				0.0000000			
ediFE_PDC6801_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:I (BUFFD3BWP35P140LVT)		0.0006183	538.5603962	0.0071530		1.0000000	0.0030720	30.1381900r
ediFE_PDC6801_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787:Z (BUFFD3BWP35P140LVT)		0.0246096	0.0000000	0.0415460		1.0765001	0.0401200	30.1783100r
FE_PDN6801_u0_soc_top_u0_spi_flash_u0_spi_top_shift_n787 (clock net)	21				0.0000000			

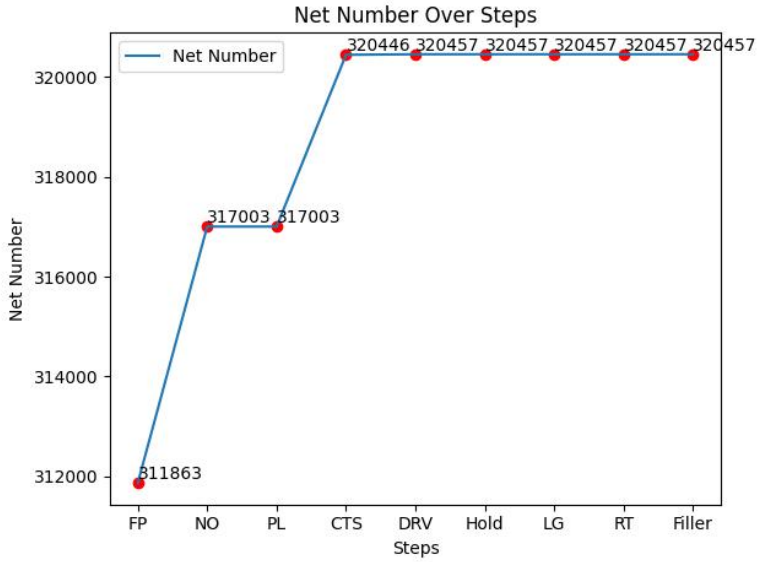
Data Analysis

Instance number



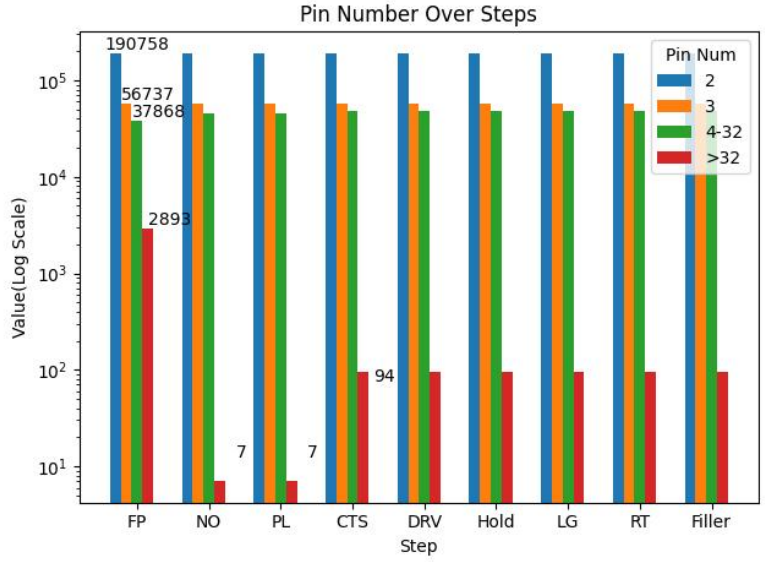
- ✓ Floorplanning -> Routing, where #Inst increased by **8594**, generated by the Fix Fanout, CTS, DRV, and Fix Setup/Hold.
- ✓ In the Filler stage, **252361** Instances is added.

Net number



- ✓ The total increase #nets in backend physical design flow is **8324**, primarily contributed by netlist optimization and clock tree synthesis stages, which are 5140 and 3284, respectively.

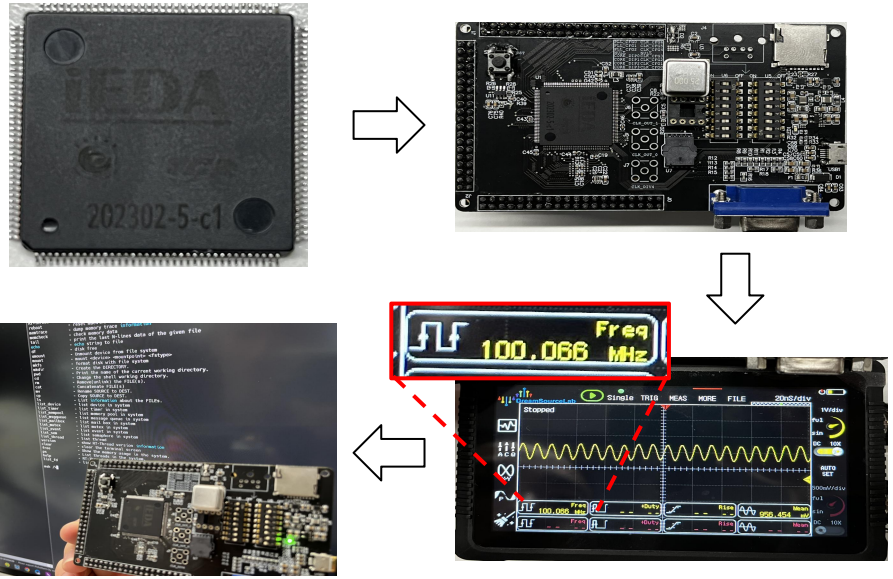
Pin number

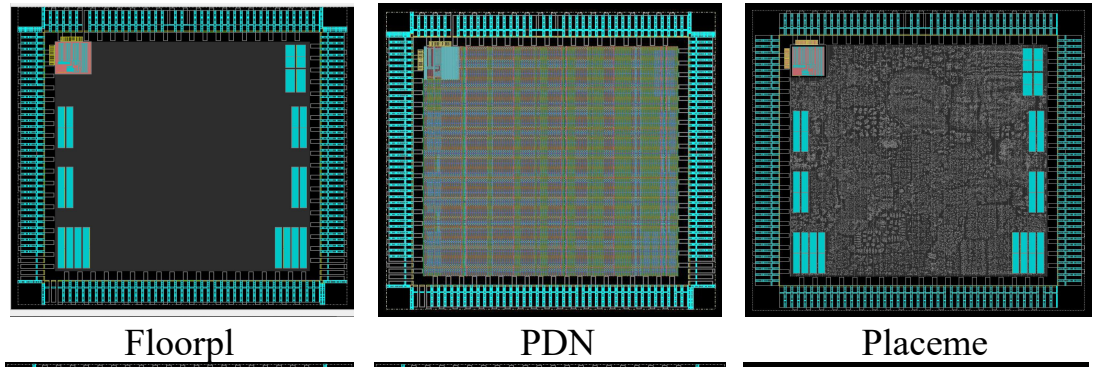


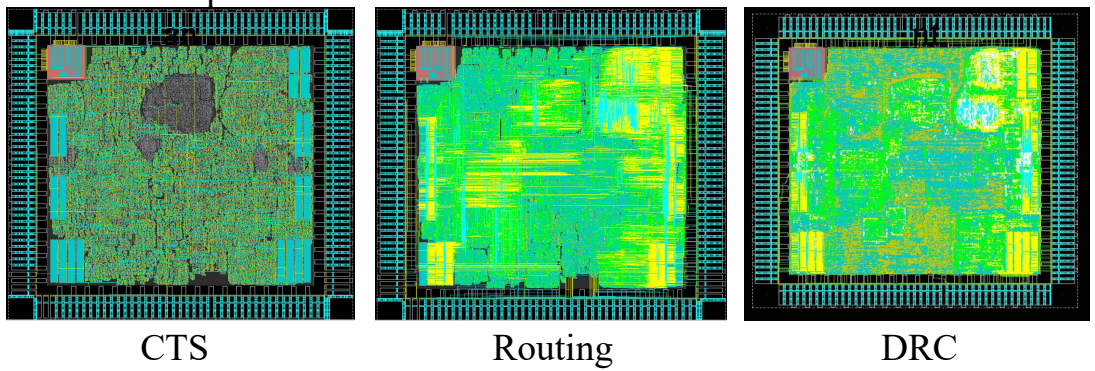
- ✓ Most of the nets consist of **2** pins and **3** pins.
- ✓ The number of nets with excessive fanout (Pins in Net) was optimized in the NO stage, reducing from **2893 to 7**.
- ✓ In the CTS stage, **87** new clock nets with excessive fanout were generated (Pin Number > 32).

Example Design: ysyx-04-01

- RTL：ysyx(一生一芯)-04
- PDK：28nm
- Area：1.5mm × 1.5 mm
- Power：dynamic = 317mW，leakage = 29 mW
- Freq.：200MHz
- Scale：>1.5M Gates
- Features：11 pipelines with cache，IP： UART、VGA、PS/2、SPI、SDRAM、 2 PLLs，support Linux







part metrics	iPL (place)	iCTS	iTO	iRT (route)
#inst	1043440	1057291	1057549	1057549
#net	1015532	1029383	1029641	1029641
utilization	0.563929	0.570644	0.570768	0.570768
HPWL	34108823398	35042653984	35044866877	50157263995*
STWL	46195026227	46580611921	46581568292	
frequency	245.245	238.226	241.386	224.254
#DRC	0	0	0	233335

* Total wirelength after routing

基于iEDA设计芯片实践

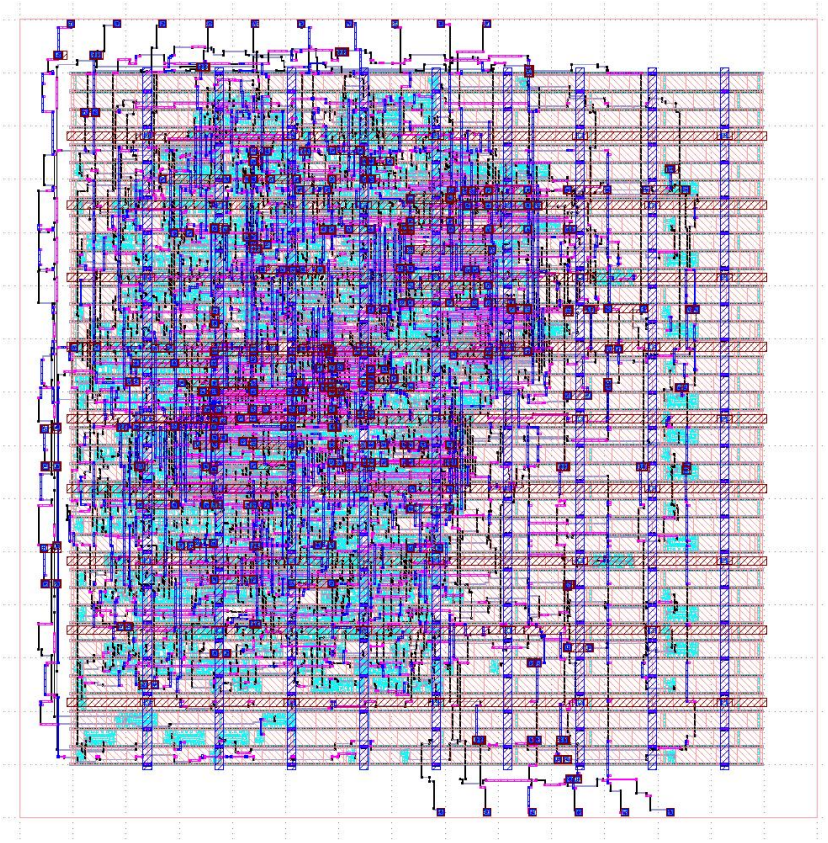
iEDA

- iEDA的Readme：
  - https://gitee.com/oscc-project/iEDA
- iEDA使用指南：
  - https://ieda.oscc.cc/tools/ieda-platform/guide.html
- iEDA安装、编译、运行视频：
  - https://www.bilibili.com/video/BV1mp4y1P7C7/?spm_id_from=333.999.0.0
- 基于iEDA的python实现RTL-to-GDS芯片设计视频：
  - https://www.bilibili.com/video/BV1Brm8YVEaY/?spm_id_from=333.999.0.0&vd_source=2ac617c241afd7f9774b0add4e647179

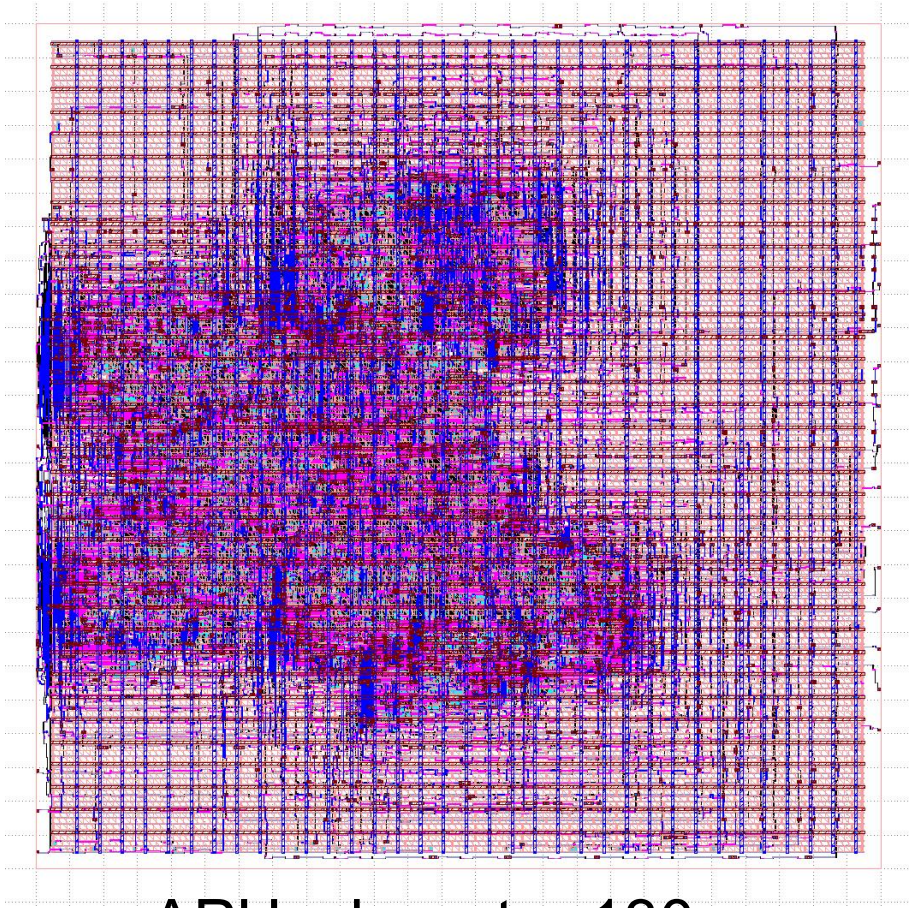
Example Design: from other users

iEDA

- gcd & APU



gcd, skywater 130nm
Area：0.15mm × 0.15 mm



APU, skywater 130nm
Area：0.45mm × 0.45 mm

R & D EDA Tools or Algorithms

iEDA

- **Min Wirelength Model**

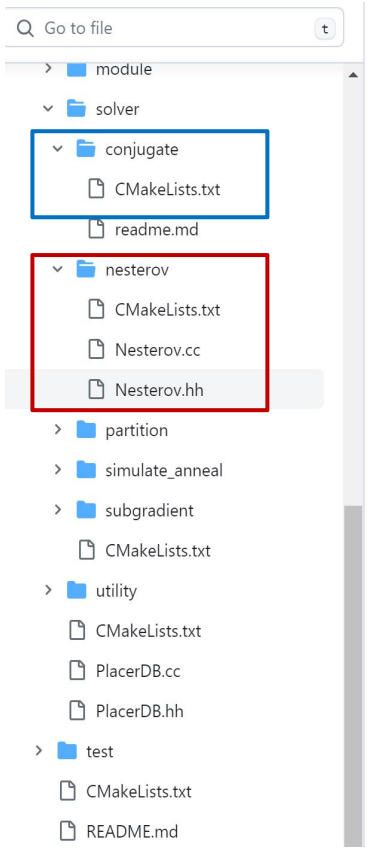
$$\min_{\boldsymbol{v}} \quad W(\boldsymbol{v})$$
$$s.t. \quad \rho_b(\boldsymbol{v}) \le \rho_0, \ \forall b \in B$$

- where v is cell location, $W(\boldsymbol{v})$ is wirelength, $\rho_b(\boldsymbol{v})$ is the area density in $b \in B$, ρ_0 is density thredhold.

- **Nesterov Method or Conjugate Gradient**

1. Given x_0, $r_0 = Ax_0 - b$, $p_0 = -r_0$
2. For $k = 0,1,2,\ldots$ until $\|r_k\| = 0$

$$\begin{aligned} \alpha_k &= r_k^T r_k / p_k^T A p_k \\ x_{k+1} &= x_k + \alpha_k p_k \\ r_{k+1} &= r_k + \alpha_k A p_k \\ \beta_{k+1} &= r_{k+1}^T r_{k+1} / r_k^T r_k \\ p_{k+1} &= -r_{k+1} + \beta_{k+1} p_k \end{aligned}$$




```
38  class Nesterov
39  {
40   public:
41    Nesterov();
42    Nesterov(const Nesterov& other) = delete;
43    Nesterov(Nesterov&& other) = delete;
44    ~Nesterov() = default;
45
46    // getter.
47    int get_current_iter() const { return _current_iter; }
48    const std::vector<Point<int32_t>>& get_current_coordis() const { return _current_coordis; }
49    const std::vector<Point<float>>& get_current_grads() const { return _current_gradients; }
50    const std::vector<Point<float>>& get_next_grads() const { return _next_gradients; }
51    const std::vector<Point<int32_t>>& get_next_coordis() const { return _next_coordis; }
52    const std::vector<Point<int32_t>>& get_next_slp_coordis() const { return _next_slp_coordis; }
53    float get_next_steplength() const { return _next_steplength; }
54
55    // for RDP
56    const std::vector<Point<float>>& get_next_gradients() const { return _next_gradients; }
57    float get_next_parameter() const { return _next_parameter; }
58    void set_next_coordis(const std::vector<Point<int32_t>>& next_coordis) { _next_coordis = next_co
59    void set_next_slp_coordis(const std::vector<Point<int32_t>>& next_slp_coordis) { _next_slp_coord
60    void set_next_gradients(const std::vector<Point<float>>& next_gradients) { _next_gradients = nex
61    void set_next_parameter(float next_parameter) { _next_parameter = next_parameter; }
62    void set_next_steplength(float next_steplength) { _next_steplength = next_steplength; }
63
64    // function.
65    void initNesterov(std::vector<Point<int32_t>> previous_coordis, std::vector<Point<float>> previo
66                      std::vector<Point<int32_t>> current_coordis, std::vector<Point<float>> current
67    void calculateNextSteplength(std::vector<Point<float>> next_grads);
68
69    void runNextIter(int next_iter, int32_t thread_num);
70    void runBackTrackIter(int32_t thread_num);
71
```

- Assignment: please implement CG method by C++ or Python, and test it on "iEDA/iPL", submit by PR to iEDA repo.

iEDA

01 Introduction

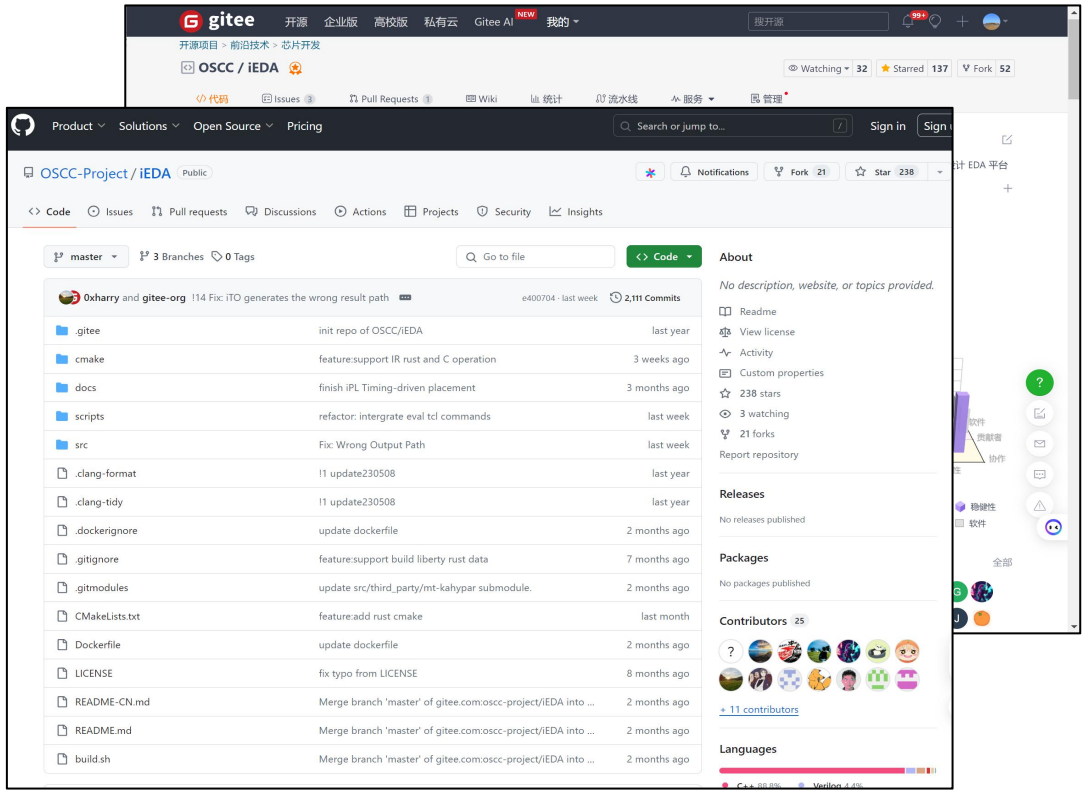
02 iEDA

03 iEDA Design Chip

04 iEDA Community

iEDA开源代码

- **Netlist-to-GDS II**
  - **11 tools，and other 5 tools are R&Ding.**
  - **Design, Analysis, Verification**
- **Repo**
  - **Gitee: https://gitee.com/oscc-project/iEDA**
  - **GitHub: https://github.com/OSCC-Project/iEDA**
  - **Gitlink: gitlink.org.cn/OSchip/iEDA**
  - **OpenI: openi.pcl.ac.cn/OSCC/iEDA**
- **Stared & Fork**
  - Stared: 238+138=**376**
  - Fork: 53+21=**74**
- **Number of Codes**
  - **>0.3M lines**
  - **exclude 3rd party and history**
- **Contributors**
  - Total: 80 contributors



Handbooks (Arxiv)

iEDA

- **Knowledge and Technology**
  - system
  - comprehensive
  - new
  - practical
  - software

iPL-1.0: An Open-source Placement EDA Tool and Its Handbook

Shijian Chen[1,4], Yihang Qiu[2], Xueyan Zhao[4], Xingquan Li[1]
[1]Peng Cheng Laboratory;
[2]University of Chinese Academy of Sciences
[4]Institute of Computing Technology, Chinese Academy of Sciences;
Email: chenshj@pcl.ac.cn, lixq01@pcl.ac.cn

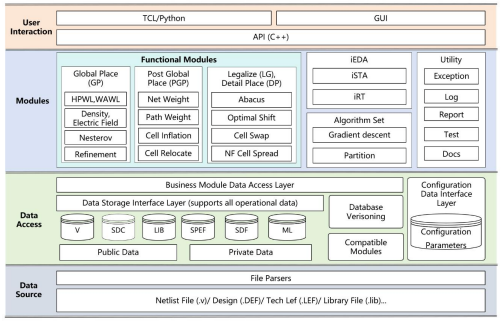


Fig. 1: **iPL: An Open-source Placement EDA Tool.** iPL is part of iEDA, it reads data from the database of iEDA into the Data Access layer, supporting common industrial standard files such as .v, .DEF, .LEF, .lib, etc., and supporting core operators including initial placement, global placement, post global placement, legalization, detailed placement, buffer insertion, filler insertion and checker. It encapsulates common utility classes like log, report, and utility, as well as math operator libraries and performance libraries, providing APIs in TCL, Python, and C++ for users.

iCTS-1.0: An Open-source Clock Tree Synthesis EDA Tool and Its Handbook

Weiguo Li[1], Xiang Cong[2], Xingquan Li[1,3]
[1]Minnan Normal University;
[2]University of Science and Technology of China;
[3]Peng Cheng Laboratory
Email: dawnli619215645@gmail.com, fzulxq@gmail.com

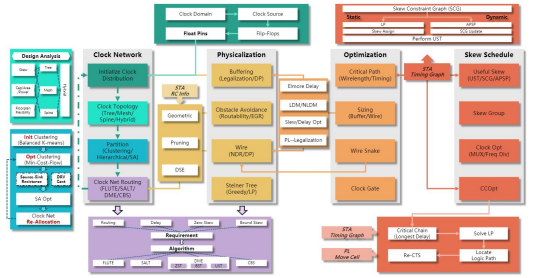


Fig. 1: **iCTS: An Open-source Clock Tree Synthesis EDA Tool.** iCTS is part of iEDA. iCTS reads data from the database of iEDA into the Data Access layer, supporting common industrial standard files such as .v, .DEF, .LEF, .lib, .spef, etc., and supporting core operators including clock topology generation, clock net routing, clock optimization and skew scheduling. It encapsulates common utility classes like log, report, and utility, as well as math operator libraries and performance libraries, providing APIs in TCL, Python, and C++ for users.

iRT-1.0: An Open-source Routing EDA Tool and Its Handbook

ZhiSheng Zeng[1], Jikang Liu[2], Kai Mo[2], Xueyan Zhao[3], Zengrong Huang[1], Xingquan Li[1]
[1]Peng Cheng Laboratory;
[2]Shenzhen University;
[3]Institute of Computing Technology, Chinese Academy of Sciences;
Email: zengzhsh@pcl.ac.cn, lixq01@pcl.ac.cn

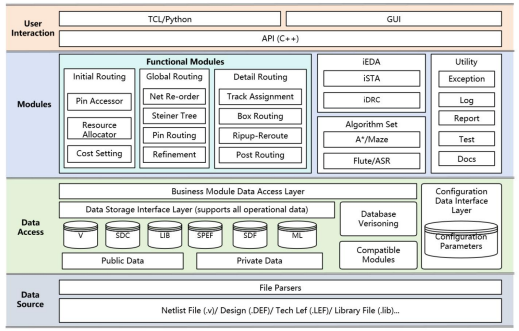


Fig. 1: **iRT: An Open-source Routing EDA Tool.** iRT is part of iEDA. iRT reads data from the database of iEDA into the Data Access layer, supporting common industrial standard files such as .v, .DEF, .LEF, .lib, .spef, etc., and supporting core operators including initial routing, global routing, track assignment, detail routing and post routing. It encapsulates common utility classes like log, report, and utility, as well as math operator libraries and performance libraries, providing APIs in TCL, Python, and C++ for users.

iSTA-1.0: An Open-source Static Timing Analysis EDA Tool and Its Handbook

Simin Tao[1], He Liu[2], Shuaiying Long[1], Xinyu Ye[3] Yingbin Cheng[4], Xingquan Li[1]
[1]Peng Cheng Laboratory;
[2]Peking University;
[3]Beijing Institute of Open Source Chip;
[4]Shanghai Tech University;
Email: taosm@pcl.ac.cn, liuh@stu.pku.edu.cn, lixq01@pcl.ac.cn

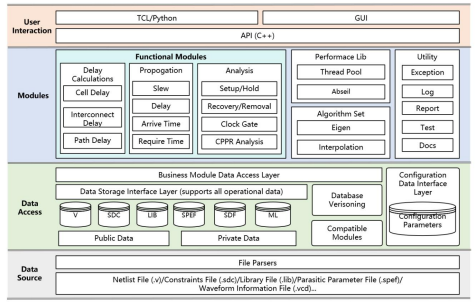


Fig. 1: **iSTA: An Open-source Static Timing Analysis EDA Tool.** iSTA is part of iEDA.iSTA reads data from the Data Source layer into the Data Access layer, supporting common industrial standard files such as .v, .sdc, .lib, .spef, .sdf, etc., and supporting core business operators including delay calculation, timing propagation, timing analysis etc. It encapsulates common utility classes like log, report, and utility, as well as math operator libraries and performance libraries, providing APIs in TCL, Python, and C++ for users.

iPA-1.0: An Open-source Power Analysis EDA Tool and Its Handbook

Simin Tao[1], Zheqing Shao[2], Xingquan Li[1]
[1]Peng Cheng Laboratory;
[2]University Science and Technology of China;
Email: taosm@pcl.ac.cn, shaozheqing@mail.ustc.edu.cn, lixq01@pcl.ac.cn

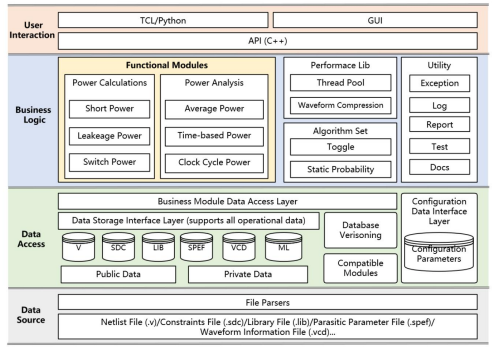
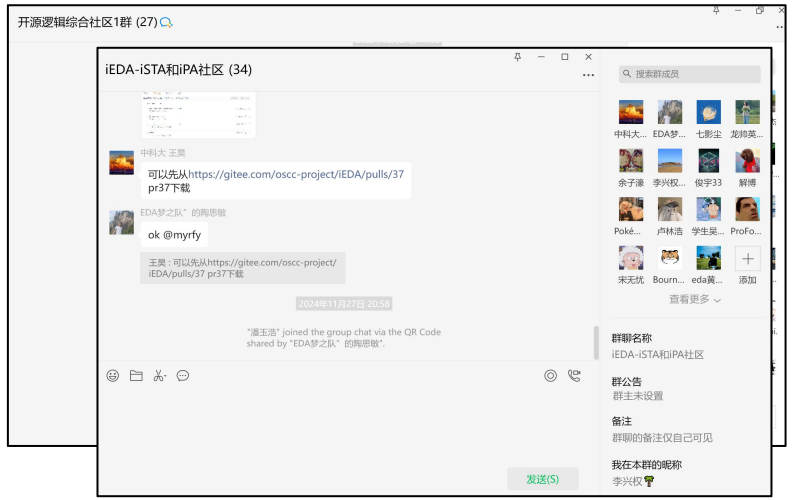


Fig. 1: **iPA: An Open-source Power Analysis EDA Tool**. iPA is part of iEDA.iPA reads data from the Data Source layer into the Data Access layer, supporting common industrial standard files such as .v, .sdc, .lib, .spef, .vcd, etc., and supporting core business operators including power calculation, power analysis, etc. It encapsulates common utility classes like log, report, and utility, as well as toggle/SP calculation algorithm libraries and performance libraries such as thread pool, and waveform compression, providing APIs in TCL, Python, and C++ for users.

Community

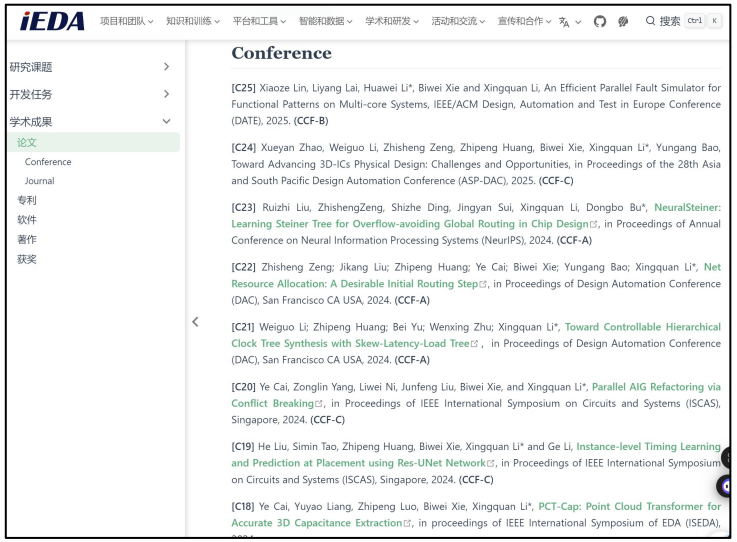
- User
  - Wechat Group
    - **>1000 Peoples**

- Contributor
  - Logic Synthesis Community；
    - Committee：ICT, Anlogic、PKU、PCL、BUPT、CUHK、Giga-da、Ninecore
  - Sign-off
    - Committee：计算所，东南大学，



iEDA网站

- iEDA website: ieda.oscc.cc

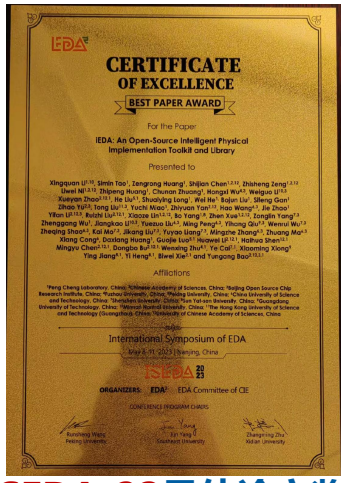


Lecture Videos (Bilibili)

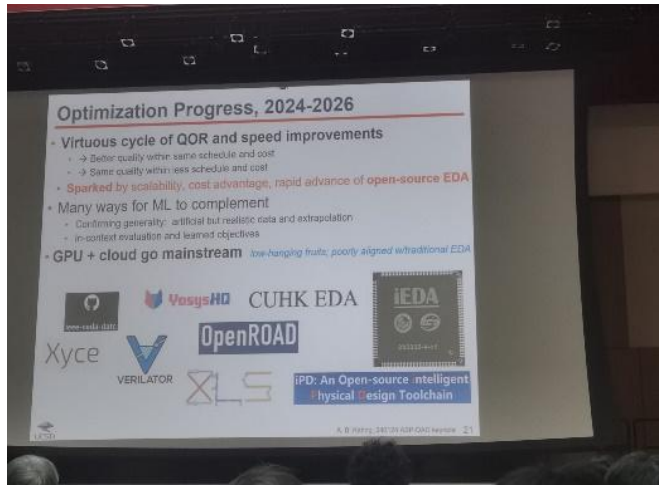
- **Lecture Videos**
  - Basic EDA Knowledge,
  - Frontiers in EDA Lectures,
  - iEDA Development Process and Tools,
  - Chip Design Using iEDA Tools,
  - Related EDA Technologies.

iEDA开源和影响

- iEDA开源项目获得500余个星，110个复制，75人代码贡献，iEDA视频获得4.5万播放量，建立包含2000人的开源EDA社区
- 支持4个EDA/芯片竞赛出题，支持5所高校课程建设，支持国内10余个EDA团队科研，支持多家EDA和芯片公司落地应用



ISEDA-23最佳论文奖



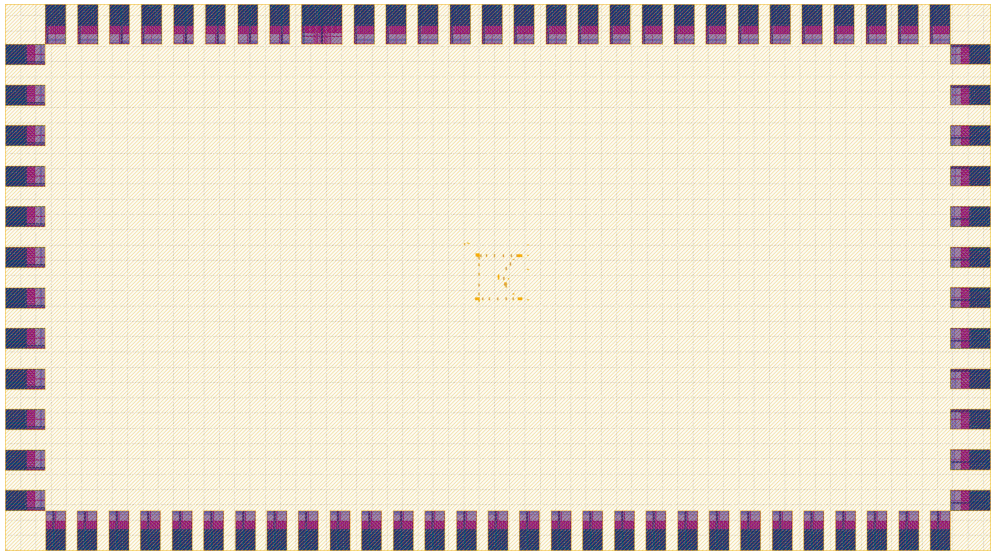
Andrew. B. Kahng（ACM/IEEE Fellow, 国际开源EDA主要推动者）
在EDA国际大会ASPDAC的主旨报告介绍iEDA

Conclusions

iEDA

- iEDA Infrastructure and Tools
  - Infras: Parser, Database, Evaluation, Manager, Interface, Solver
  - Tools: iMap, iFP, iNO, iPL, iCTS, iRT, iSTA, iTO, iPA, iDRC
- iEDA Chip Design
  - iEDA Flow
  - Chip Design
- iEDA Community
  - Code Repos
  - Website
  - iEDA Handbook (arxiv)
  - Wechat Group
  - iEDA-Videos

iEDA



Thanks

iEDA website: ieda.oscc.cc

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fzulxq@gmail.com