物理设计

设计流程基础

李兴权

iEDA

iEDA

01 基础介绍

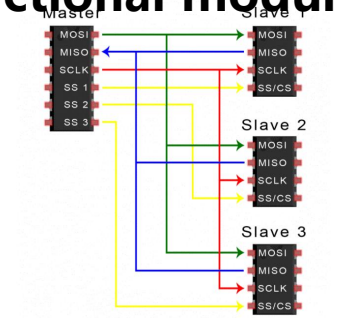
02 相关文件

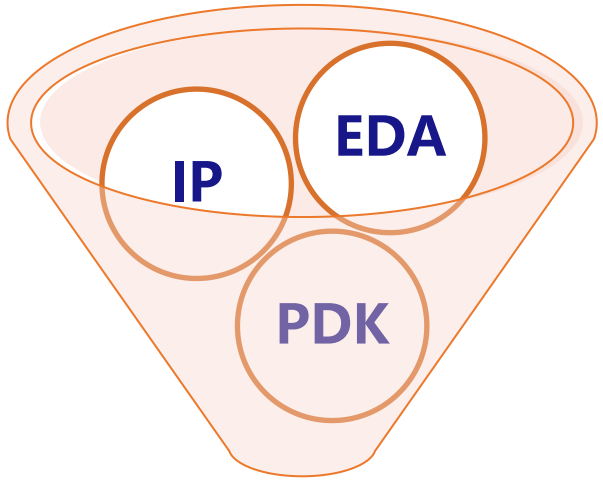
03 主要步骤

集成电路设计基本要素

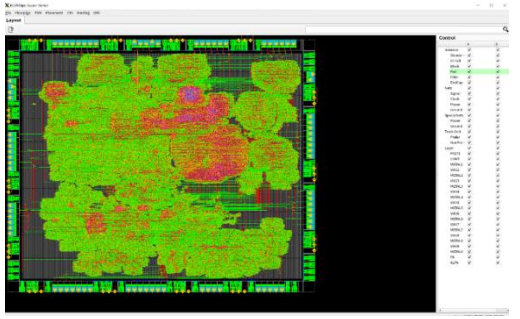
iEDA

IP：**Intellectual Property**
Functional module

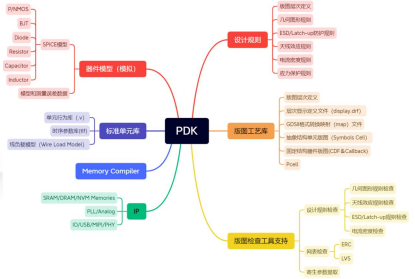




EDA：**Electronic design automation software (tool)**

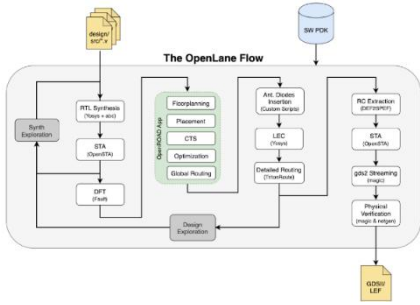


PDK：**Process design kits from foundary**



Flow

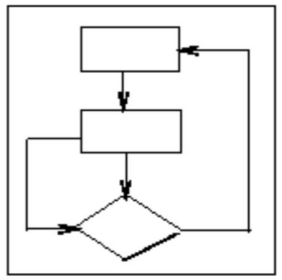
Flow：**Chip design flow config and script**

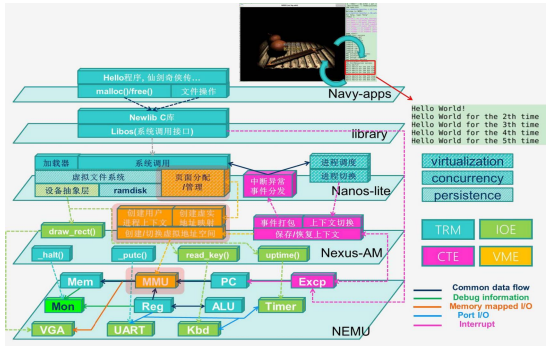


数字芯片设计流程

- **EDA工具全程自动化支持芯片设计、验证和测试**

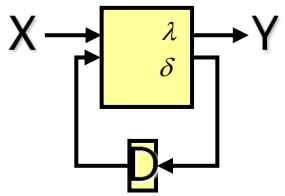
系统规格定制 → 架构设计 → 功能开发 → 逻辑综合 → 工艺映射

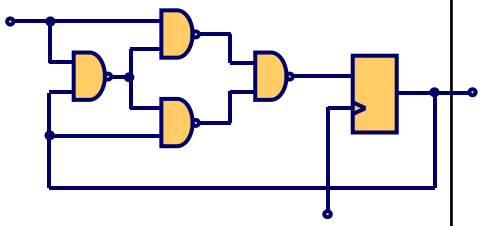




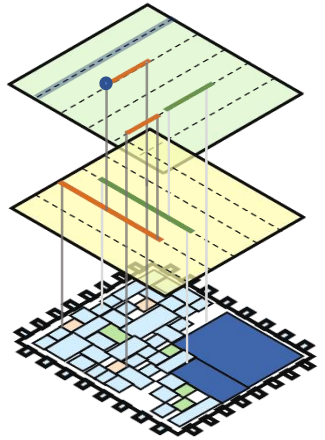

```
module conv;
reg [31:0] m[0:8192];
reg [12:0] pc;
reg [31:0] acc;
reg[15:0] ir;

always
  begin
    ir = m[pc];
    if(ir[15:13] == 3b’ 000)
      pc = m[ir[12:0]];
    else if (ir[15:13] == 3’ b010)
      acc = -m[ir[12:0]];
    ...
```

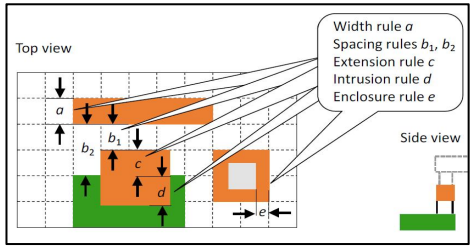


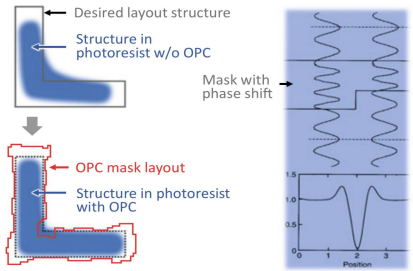


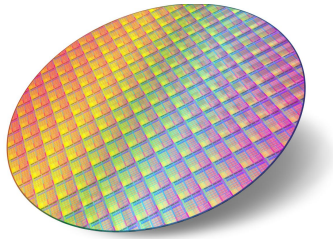
物理设计 → 签核验证 → 版图综合 → 制造 → 封装测试



时序, 功耗, DRC, ERC, LVS







物理设计流程

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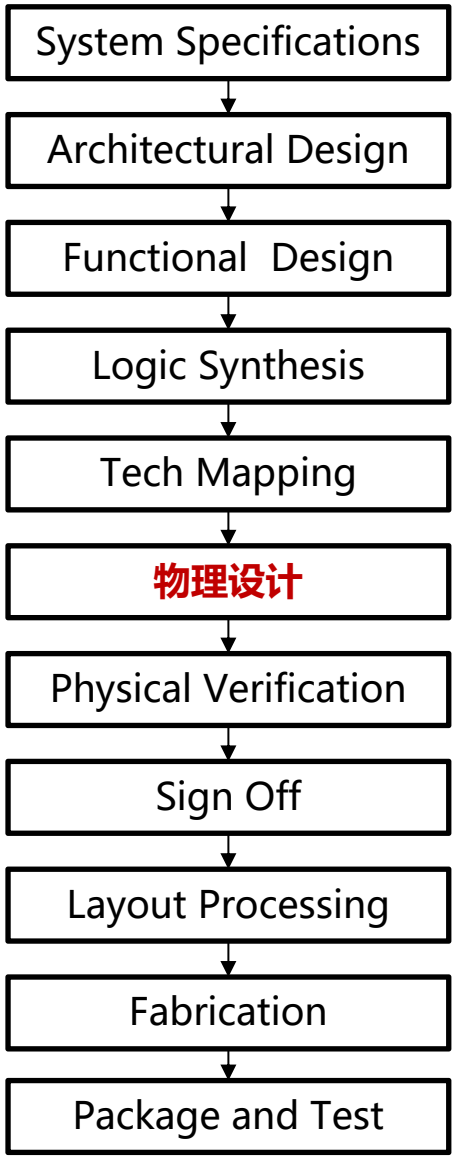
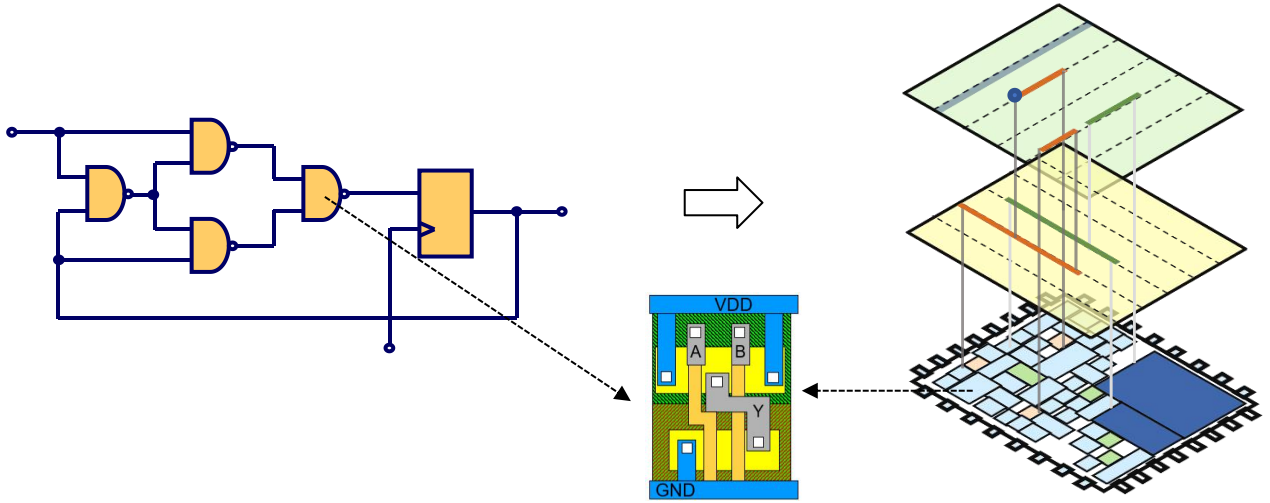
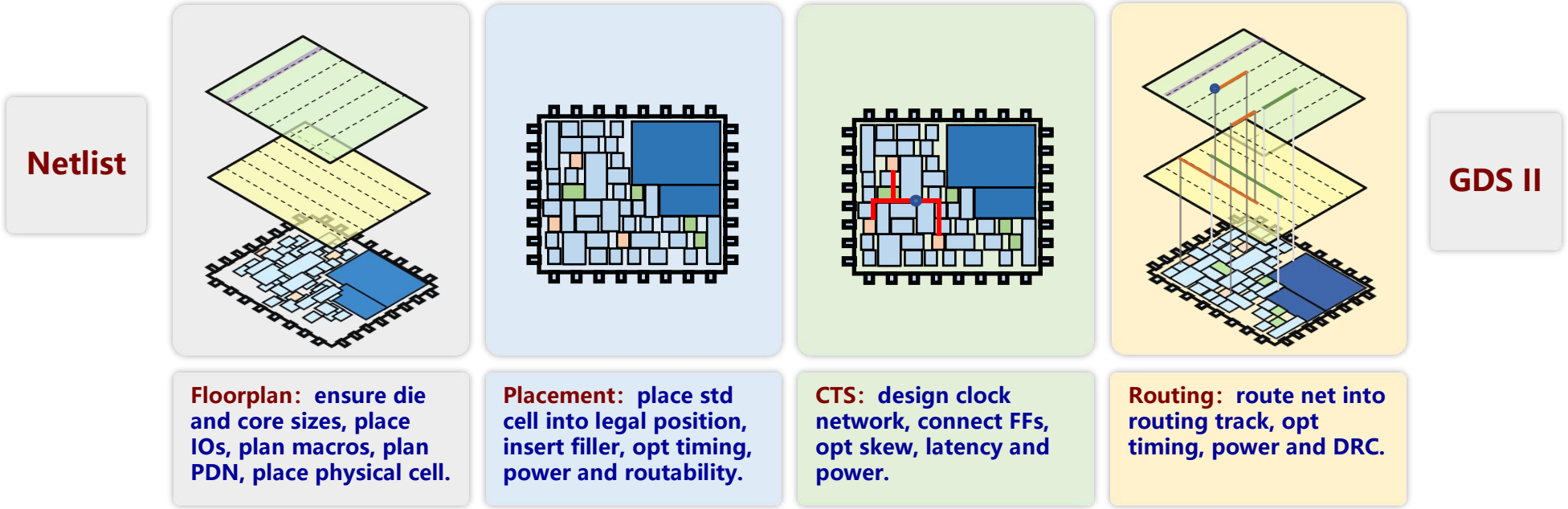


- **物理设计**
  - converts a **circuit（电路）** description into a **geometric（几何版图）** description, optimize **Performance、Power、Area** (性能，功耗，面积)
- **主要步骤**
  - **floorplan（布图规划），placement（布局），clock tree synthesis (CTS, 时钟树综合), routing（布线）**
- **其他步骤**
  - 划分, 时序优化,
  - 静态时序分析（STA），功耗分析，寄生参数提取，电压降，电迁移
  - 设计规则检查（DRC），版图原理图对比（LVS），...



物理设计流程

- **物理设计:** converts a **circuit（电路）** description into a **geometric（几何版图）** description, optimize **Performance、Power、Area** (性能，功耗，面积)



Standard Cell Library（标准单元库）

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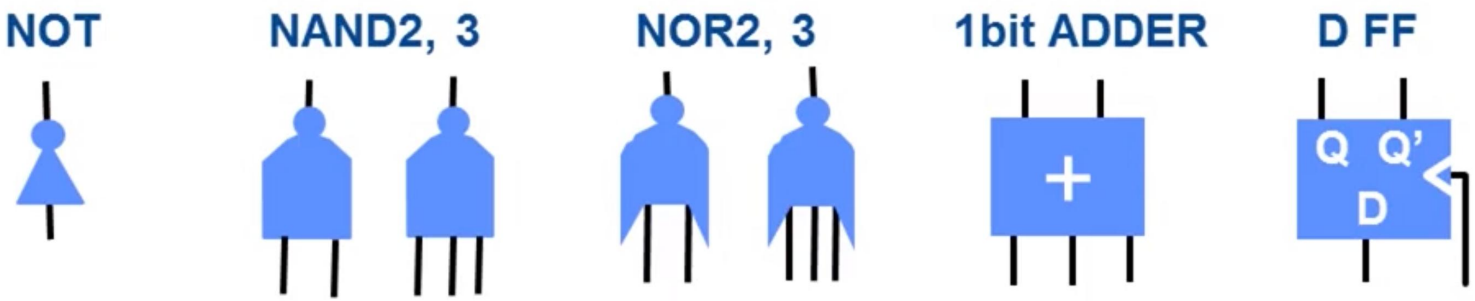
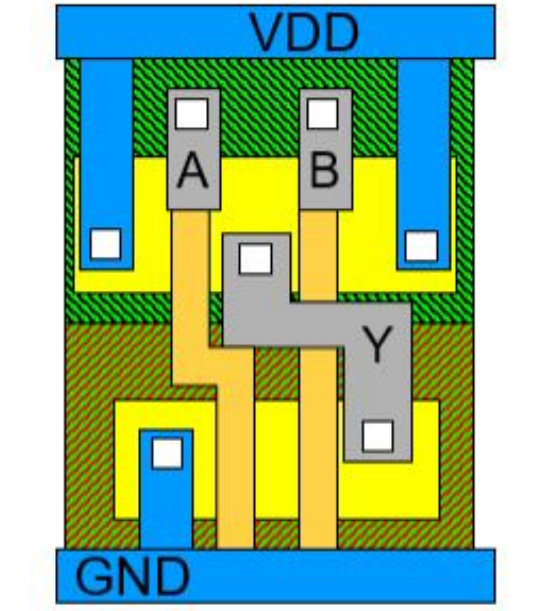
- A Standard Cell is a predesigned layout of one specific basic logic gate
  - Each cell usually has the same standard height.
  - A Standard Cell Library contains a varied collection of standard cells
  - Libraries are usually supplied by an ASICvendor or library group





Layout View

2-Input NAND Gate

Standard Cell Library（标准单元库）

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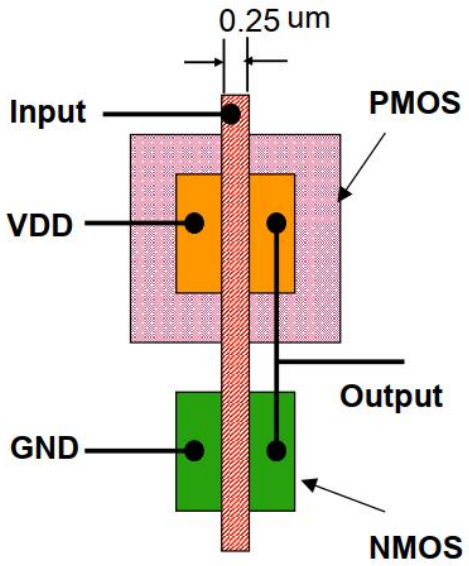
- Often,very big
  - For all logic functions, input/output variants,timing variants,electrical drive strengths

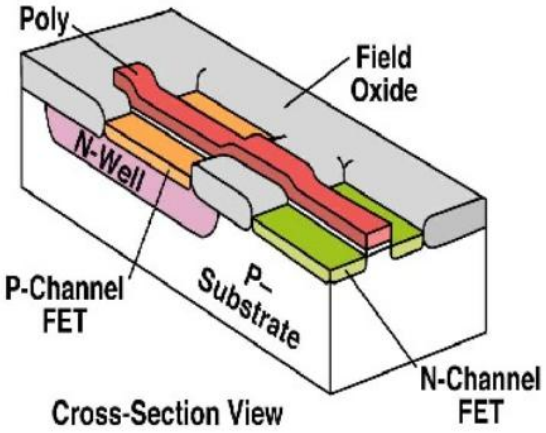
- How to think about a standard cell
  - Simple abstraction of a geometric “container" for the circuits you need to make logic.
  - Inside the cellComplex device & mask & electrical issues
  - Outside the cell: A box with pins

标准单元几何形状

- Example of complimentary devices in 110nm CMOS technology or process.



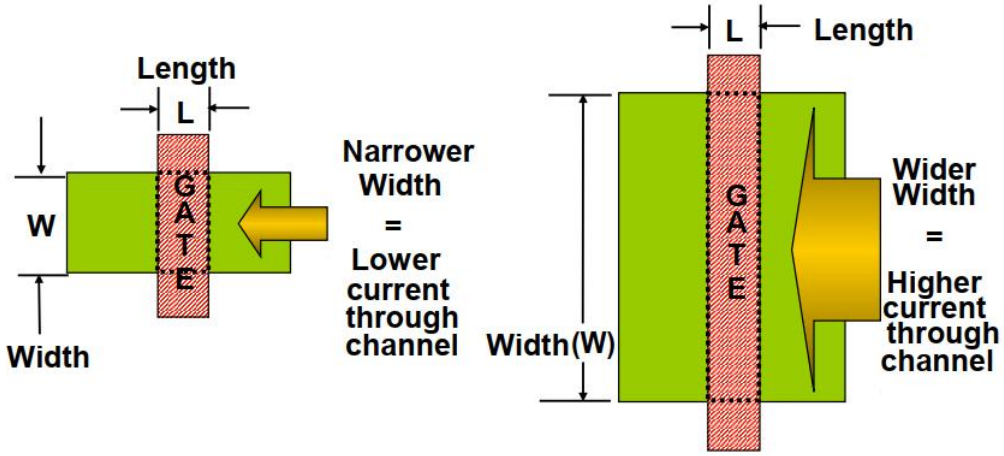
Aerial or Layout View



Wafer Cross-sectional View

工艺节点（**nm工艺）

- Gate or Channel Dimensions (L and W)

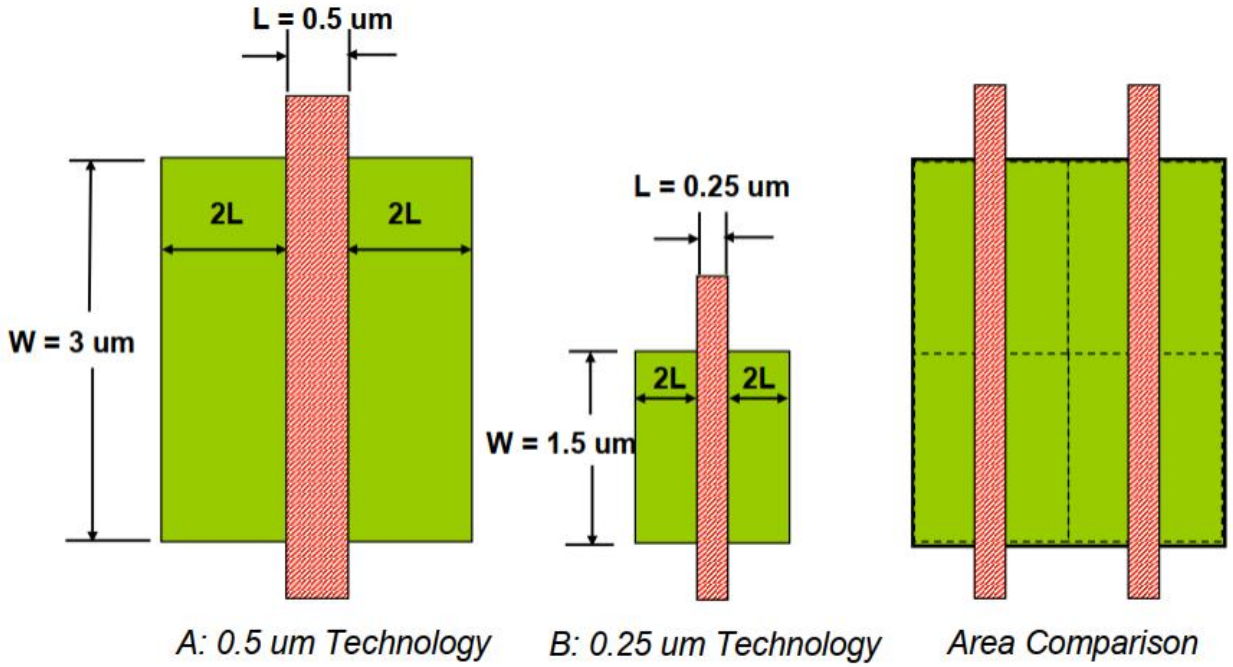


**nm Technology

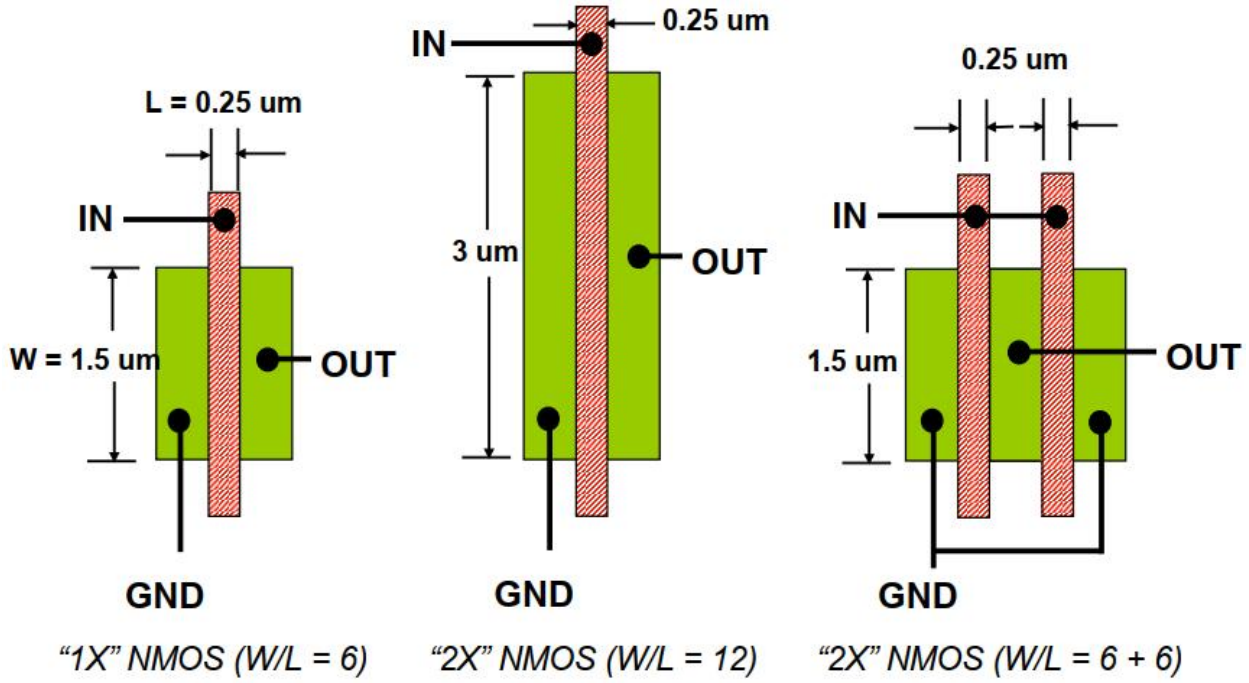
- In CMOS Technology the um or nm dimension refers to the channel length, a minimum dimension which is fixed for most devices in the same library.
- Current flow or drive strength of the device is proportional to W/L; Device size or area is proportional to W x L.

工艺对比

- The drive strength of both devices is the same: W/L = 6.
- The diffusion area (5xLxW) of A is 4x that of B.
- Which is preferred?



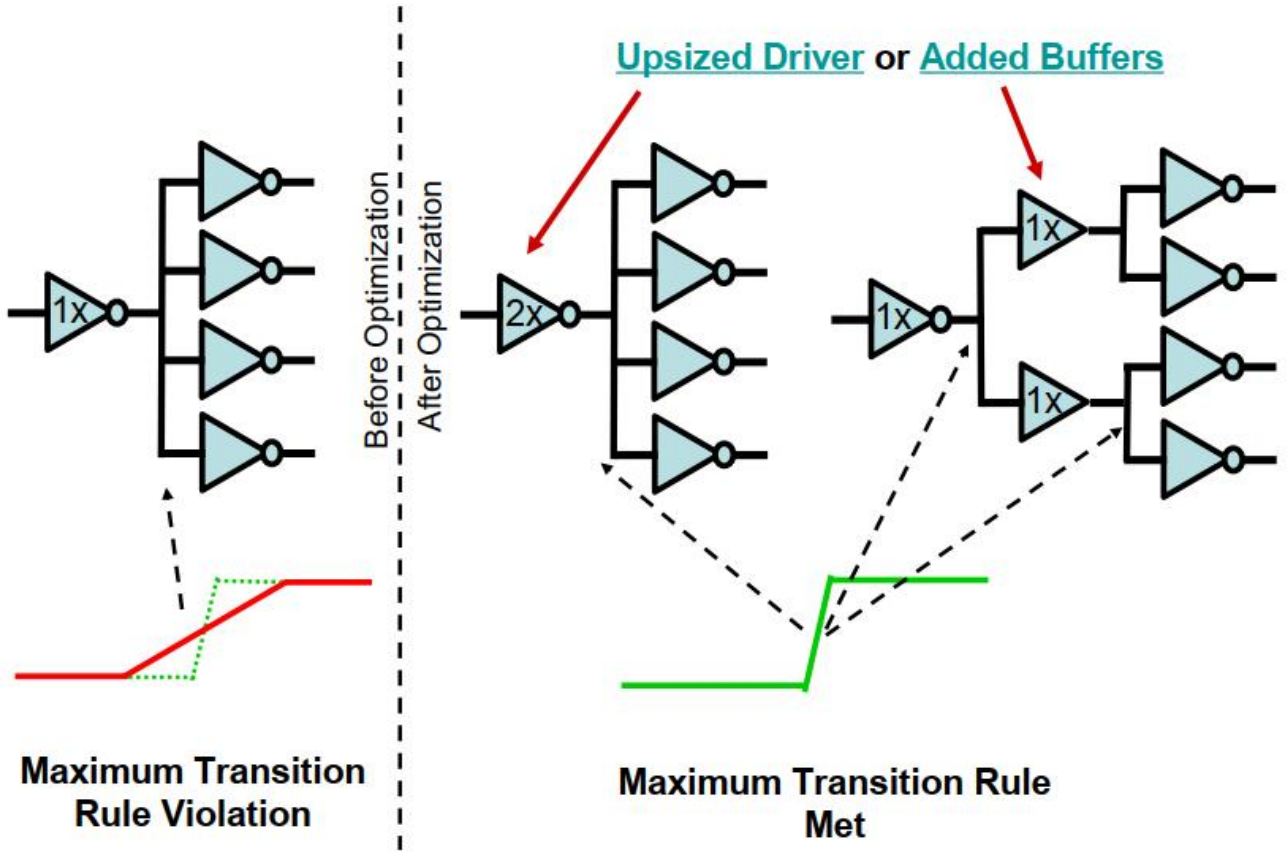
驱动强度



Drive Strengths

To double the drive strength of a device, double the channel width (W), or connect two 1X devices in parallel. The latter approachkeeps the height at a fixed or "standard" height.

驱动规则: Max Transition/Cap



Gate（门）

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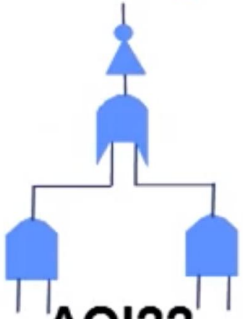
- **Strange question: How big is a “100 million gate ASIC”**
  - Surprisingly, it is almost certainly **NOT** 100,000,000 logic gates
  - Numbers are usually “equivalent small gates” – transform all logic into **2-input NANDs**

Size? 1 gate

NAND2

Size? ~4 gates

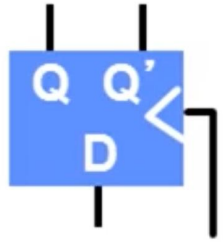


AOI22

Size? ~6 gates

1bit adder

Size? ~10 gates



D Flip Flop

- **Consequence: 2 measures people use for “size” here**
  - **Gates**: This is “equivalent little NAND gates”. Usually a big number
  - **Instances**: # things *really* placed. **~Rule: Instances = Gates ÷ 4 or 5**

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01 基础介绍

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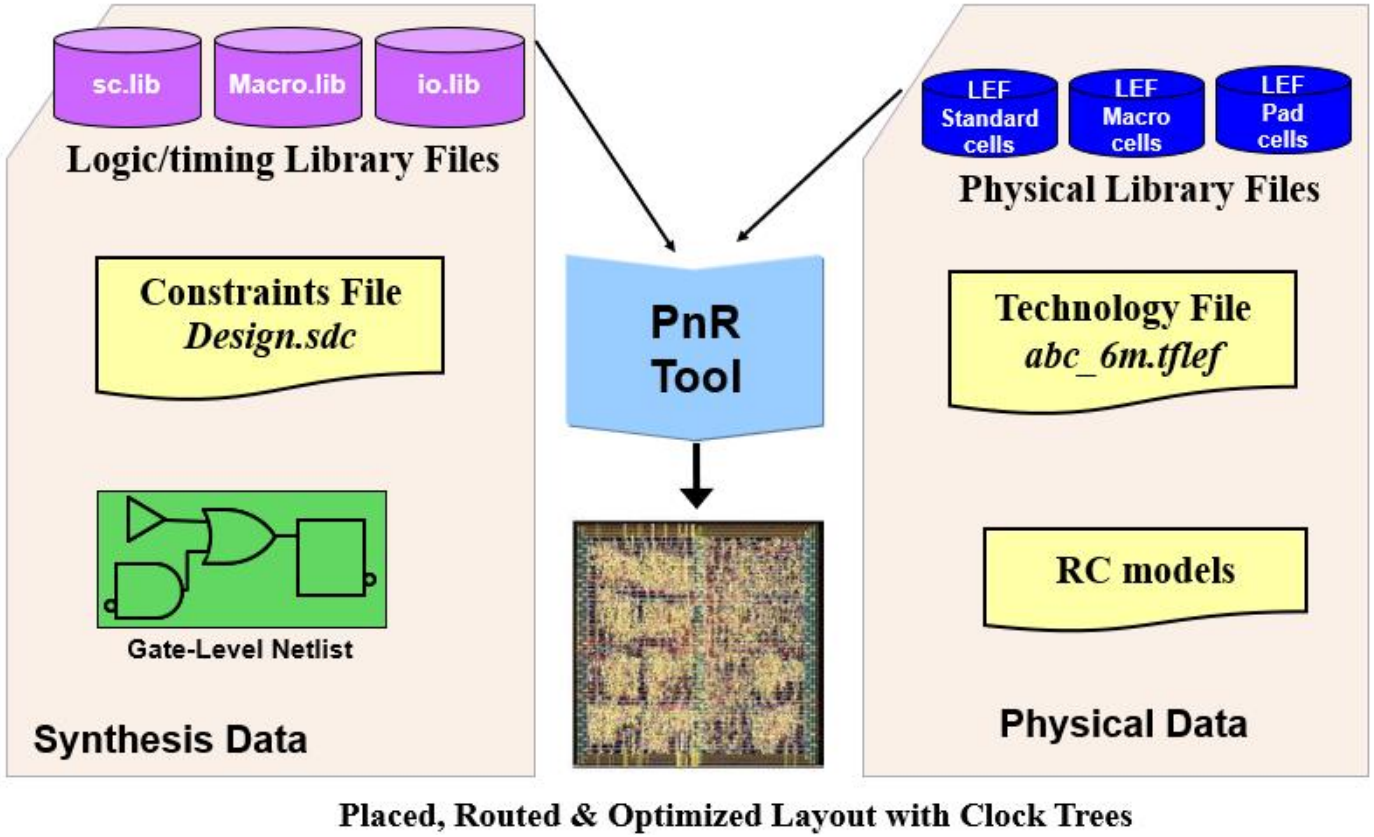
03 主要步骤

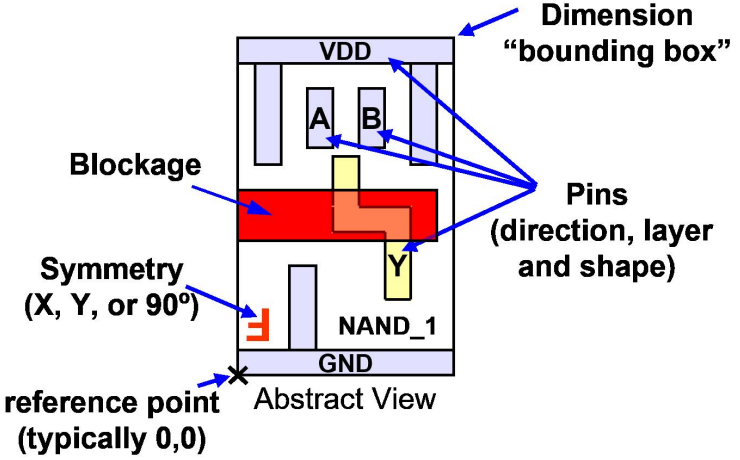
输出数据文件

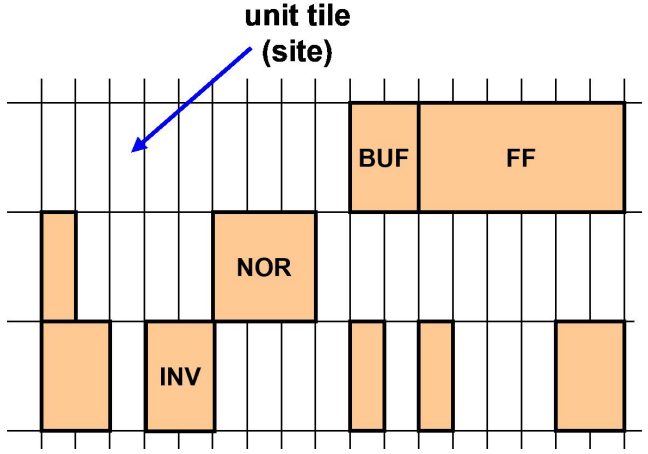
- **Input Files**
  - Physical Libraries (.lef)
  - Liberty (.lib)
  - Timing Constraints (.sdc)
  - Technology Files (.tf, .itf)



Physical Libraries (.LEF)

- Contain physical information of standard, macro and pad cells, necessary for placement and routing
- Define placement unit tile
  - Height of placement rows
  - Minimum width resolution
  - Preferred routing directions
  - Pitch of routing tracks

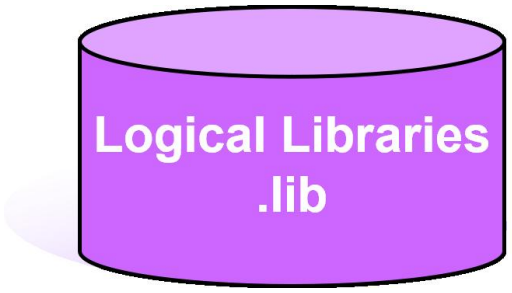





```
MACRO sky130_fd_sc_hd__clkinv_2
  CLASS CORE ;
  ORIGIN  0.000000  0.000000 ;
  SIZE  1.840000 BY  2.720000 ;
  SYMMETRY X Y R90 ;
  SITE unithd ;
  PIN A
    ANTENNAGATEAREA  0.576000 ;
    DIRECTION INPUT ;
    USE SIGNAL ;
    PORT
      LAYER li1 ;
        RECT 0.085000 1.065000 1.305000 1.290000 ;
    END
  END A
  PIN Y
    ANTENNADIFFAREA  0.662600 ;
    DIRECTION OUTPUT ;
    USE SIGNAL ;
    PORT
      LAYER li1 ;
        RECT 0.155000 1.460000 1.755000 1.630000 ;
        RECT 0.155000 1.630000 0.410000 2.435000 ;
        RECT 1.010000 1.630000 1.270000 2.435000 ;
        RECT 1.025000 0.280000 1.250000 0.725000 ;
        RECT 1.025000 0.725000 1.755000 0.895000 ;
        RECT 1.475000 0.895000 1.755000 1.460000 ;
    END
  END Y
  PIN VGND
    DIRECTION INOUT ;
    SHAPE ABUTMENT ;
    USE GROUND ;
    PORT
      LAYER li1 ;
        RECT 0.000000 -0.085000 1.840000 0.085000 ;
        RECT 0.560000  0.085000 0.855000 0.610000 ;
        RECT 1.420000  0.085000 1.750000 0.555000 ;
    END
    PORT
      LAYER met1 ;
        RECT 0.000000 -0.240000 1.840000 0.240000 ;
    END
  END VGND
  PIN VPWR
    DIRECTION INOUT ;
    SHAPE ABUTMENT ;
    USE POWER ;
    PORT
      LAYER li1 ;
        RECT 0.000000 2.635000 1.840000 2.805000 ;
        RECT 0.580000 1.800000 0.840000 2.635000 ;
        RECT 1.440000 1.800000 1.695000 2.635000 ;
    END
    PORT
      LAYER met1 ;
        RECT 0.000000 2.480000 1.840000 2.960000 ;
    END
  END VPWR
  OBS
  END
END sky130_fd_sc_hd__clkinv_2
```

Liberty (.lib)

- Provide timing and functionality information for all standard cells
  - (inv, and, or, flipflop, ...)
- Provide timing information for hard macros(IP, ROM, RAM, ...)
- Define drive/load design rules:
  - Max fanout
  - Max transition
  - Max/Min capacitance
- Are usually the same ones used by Syntheis during synthesis




```
cell ("sky130_fd_sc_hs__a211oi_1") {
    leakage_power () {
        value : 0.1807600000;
        when : "!A1&!A2&!B1&!C1";
    }
    leakage_power () {
        value : 9.4646600000;
        when : "!A1&!A2&!B1&C1";
    }
    leakage_power () {
        value : 2.4273000000;
        when : "!A1&!A2&B1&!C1";
    }
    leakage_power () {
        value : 0.1226900000;
        when : "!A1&!A2&B1&C1";
    }
    leakage_power () {
        value : 0.2575600000;
        when : "!A1&A2&!B1&!C1";
    }
    leakage_power () {
        value : 9.4630400000;
        when : "!A1&A2&!B1&C1";
    }
    leakage_power () {
        value : 2.4273100000;
        when : "!A1&A2&B1&!C1";
    }
    leakage_power () {
        value : 0.1226900000;
        when : "!A1&A2&B1&C1";
    }
    leakage_power () {
        value : 0.2317100000;
        when : "A1&!A2&!B1&!C1";
    }
    leakage_power () {
        value : 9.4626800000;
        when : "A1&!A2&!B1&C1";
    }
    leakage_power () {
```

Timing Constraints（.sdc)

- “Timing Constraints” are required to communicate the design’s timing intentions to PnR Tool
- They should be the same ones used for synthesis with Synthesis Tool (preferably SDC)

```
create_clock -period 10 [get_ports clk]
set_input_delay 4 -clock clk \
        [get_ports sd_DQ[*]]
set_output_delay 5 -clock clk
        [get_ports sd_LD]
set_load 0.2 [get_ports pdevsel_n]
set_driving_cell -lib_cell buf5 \
        [get_ports pdevsel_n]
...
```

```
1  #current_design gcd
2
3  set clk_name  core_clock
4  set clk_port_name clk
5  set clk_period 2.0
6  set clk_io_pct 0.2
7
8  set clk_port [get_ports $clk_port_name]
9
10 create_clock -name $clk_name -period $clk_period  $clk_port
11
```

Technology File (.tf lef file)

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- Tech File is unique to each technology
- Contains metal layer technology parameters:
  - Number and name designations for each layer/via
  - Dielectric constant for technology
  - Physical and electrical characteristics of each layer/via
  - Design rules for each layer/Via (Minimum wire widths and
  - wire-to-wire spacing, etc.)
  - Units and precision for electrical units
  - Colors and patterns of layers for display
  - ....

abc_6m.tf

```
Technology  {
        dielectric              = 3.7
        unitTimeName            = "ns"
        timePrecision           = 1000
        unitLengthName          = "micron"
        lengthPrecision         = 1000
        gridResolution          = 5
        unitVoltageName         = "v"
        }
...
Layer  "m1" {
        layerNumber             = 16
        maskName                = "metal1"
        pitch                   = 0.56
        defaultWidth            = 0.23
        minWidth                = 0.23
        minSpacing              = 0.23
        ...
```

Design File (.def)

- Design File是用来描述芯片版图信息
  - Die area
  - Row，行
  - Tracks，轨道
  - GCell Grid，网格
  - Components，标准单元
  - Nets，线网
  - Special Nets，特殊线网

```
VERSION 5.8 ;
DIVIDERCHAR "/" ;
BUSBITCHARS "[]" ;
DESIGN gcd ;
UNITS DISTANCE MICRONS 2000 ;

PROPERTYDEFINITIONS
    DESIGN ER_routing_mode STRING "trial_opt" ;
    DESIGN flow_implementation_stage STRING "postcts" ;
    NET StnRoutedCapScaleProp REAL ;
    NET StnRoutedResScaleProp REAL ;
    COMPONENTPIN designRuleWidth REAL ;
    DESIGN FE_CORE_BOX_LL_X REAL 0.9800 ;
    DESIGN FE_CORE_BOX_UR_X REAL 20.0200 ;
    DESIGN FE_CORE_BOX_LL_Y REAL 1.0000 ;
    DESIGN FE_CORE_BOX_UR_Y REAL 20.0000 ;
END PROPERTYDEFINITIONS

DIEAREA ( 0 0 ) ( 42000 42000 ) ;

ROW ROW_0 core 1960 2000 FS DO 136 BY 1 STEP 280 0
 ;
ROW ROW_1 core 1960 3800 N DO 136 BY 1 STEP 280 0
 ;
ROW ROW_2 core 1960 5600 FS DO 136 BY 1 STEP 280 0
 ;
ROW ROW_3 core 1960 7400 N DO 136 BY 1 STEP 280 0
 ;
```

```
TRACKS Y 200 DO 209 STEP 200 LAYER M6 ;
TRACKS Y 200 DO 209 STEP 200 LAYER M5 ;
TRACKS X 160 DO 210 STEP 200 LAYER M5 ;
TRACKS X 160 DO 210 STEP 200 LAYER M4 ;
TRACKS Y 200 DO 209 STEP 200 LAYER M4 ;
TRACKS Y 200 DO 209 STEP 200 LAYER M3 ;
TRACKS X 160 DO 210 STEP 200 LAYER M3 ;
TRACKS X 160 DO 210 STEP 200 LAYER M2 ;
TRACKS Y 200 DO 209 STEP 200 LAYER M2 ;
TRACKS Y 200 DO 209 STEP 200 LAYER M1 ;
TRACKS X 140 DO 150 STEP 280 LAYER M1 ;

GCELLGRID Y 42010 DO 1 STEP 2910 ;
GCELLGRID Y 6100 DO 12 STEP 3000 ;
GCELLGRID Y -10 DO 2 STEP 3110 ;
GCELLGRID X 42010 DO 1 STEP 2970 ;
GCELLGRID X 6040 DO 12 STEP 3000 ;
GCELLGRID X -10 DO 2 STEP 3050 ;

VIAS 13 ;
- VIAGEN89_1
 + VIARULE VIAGEN89
 + CUTSIZE 720 720
 + LAYERS M8 VIA8 M9
 + CUTSPACING 1080 1080
 + ENCLOSURE 160 40 40 160
 + ROWCOL 5 5
```

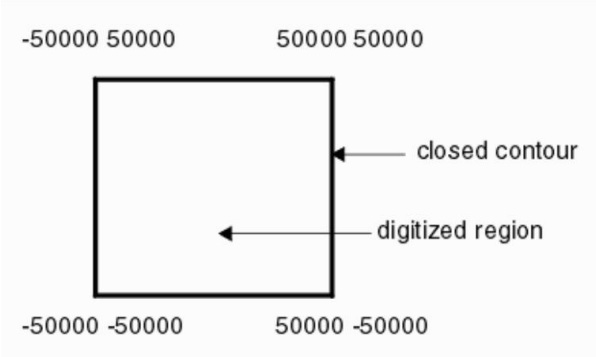
```
COMPONENTS 297 ;
- CTS_ccl_a_buf_00004 CKBD4BWP35P140 + PLACED ( 4200 14600 ) FN + WEIGHT 1
 ;
- ctrl/placeFE_OFC1_ctrl_b_mux_sel_0 BUFFD3BWP30P140LVT + PLACED ( 5880 20000 ) S
 ;
- ctrl/U3 AOI21D1BWP40P140 + PLACED ( 10080 18200 ) FN
 ;
- ctrl/U4 INVD3BWP30P140LVT + PLACED ( 10360 16400 ) FS
 ;
- ctrl/U5 NR2D1BWP40P140 + PLACED ( 7280 20000 ) FS
 ;
- ctrl/U7 BUFFD3BWP40P140 + PLACED ( 3920 5600 ) S
 ;
- ctrl/U8 ND2D1BWP40P140 + PLACED ( 10080 20000 ) FS
 ;
- ctrl/U9 NR2D1BWP40P140 + PLACED ( 9240 21800 ) FN
 ;
- ctrl/U10 AOI21D1BWP40P140 + PLACED ( 8680 12800 ) S
 ;
- ctrl/U11 AOI21D1BWP40P140 + PLACED ( 7840 18200 ) N
 ;
- ctrl/U12 INVD1BWP40P140 + PLACED ( 11200 18200 ) N
 ;
```

```
    NEW M8 0 + SHAPE STRIPE ( 8260 33200 ) VIAGEN78_1
    NEW M8 0 + SHAPE STRIPE ( 28260 14000 ) VIAGEN78_1
    NEW M8 0 + SHAPE STRIPE ( 28260 33200 ) VIAGEN78_1
  + USE GROUND
 ;
- VDDIO
  + USE POWER
 ;
- POC
  + USE POWER
 ;
- VSSIO
  + USE GROUND
 ;
END SPECIALNETS

NETS 270 ;
- dpath/CTS_1
  ( dpath/CTS_ccl_a_buf_00006 Z ) ( dpath/a_reg/out_reg_12_ CP )
  ( dpath/a_reg/out_reg_11_ CP ) ( dpath/a_reg/out_reg_9_ CP )
  ( dpath/a_reg/out_reg_8_ CP ) ( dpath/a_reg/out_reg_7_ CP )
  ( dpath/a_reg/out_reg_6_ CP ) ( dpath/a_reg/out_reg_5_ CP )
```

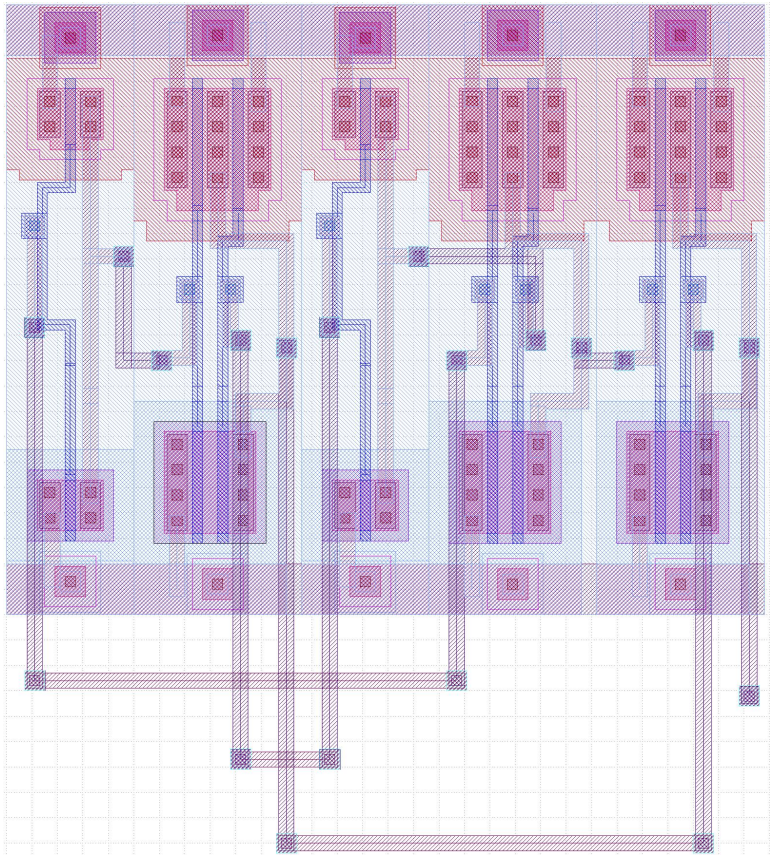
Graphic Design System II (.gdsii)

- GDS是最后的几何形状文件，
  - 交给芯片生产厂的文件




```
BOUNDARY 5 0  <-- layer 5, datatype 0
-50000 -50000 <-- First X,Y vertex
50000 -50000  <-- Second X,Y vertex
50000 50000   <-- Third X,Y vertex
-50000 50000  <-- Fourth X,Y vertex
-50000 -50000 <-- Back to First X,Y vertex
ENDEL
```

[Note: Since this example assumes units of UM and a resolution of 1000 UM per GDSII db tick, each integer value is 1000x the value in UM]



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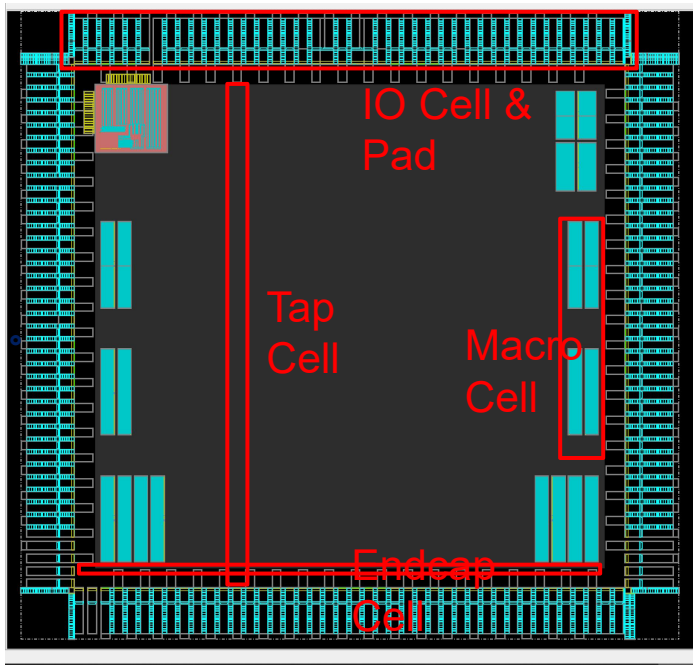
01 基础介绍

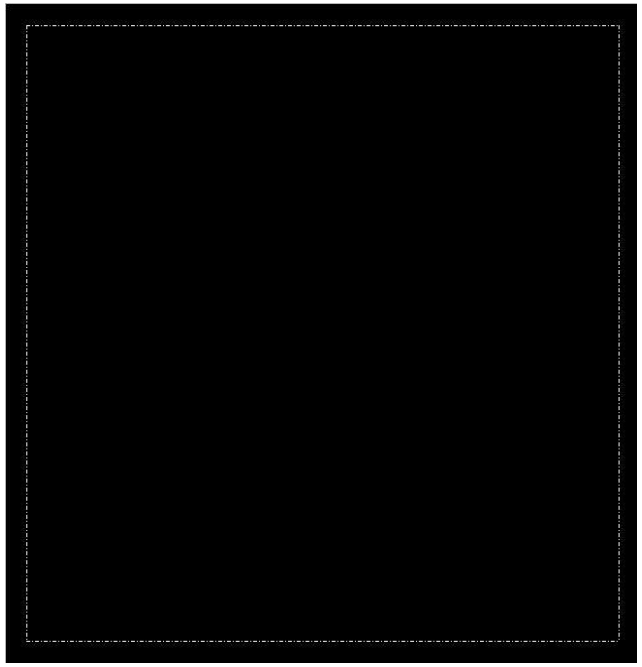
02 相关文件

03 主要步骤

Floorplanning（布图规划）

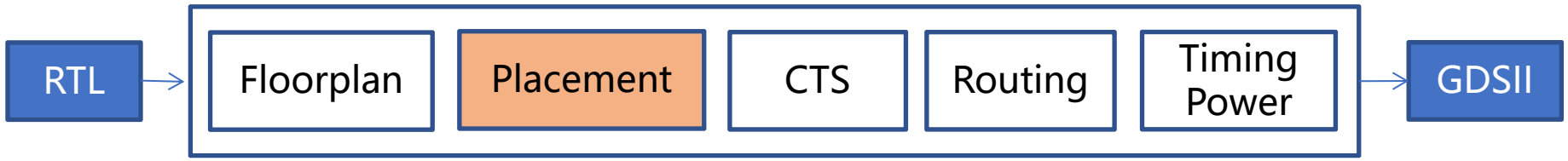
- 布图规划（Floorplanning）是逻辑描述（网表）和物理描述（楼层平面图）之间的映射。
- 任务：
  - 1. 定义芯片尺寸和核心区域尺寸。
  - 2. 确定 I/O 引脚的位置。
  - 3. 确定宏单元（模块）的放置位置。
  - 4. 决定电源网络及过孔/引脚设计。
  - 5. 定义电源域。
  - 6. 放置物理单元（如 tap cell、endcap 等）
- 目标：
  - - 最小化芯片面积
  - - 最小化延迟
  - - 最小化布线拥堵
- 概念：
  - - 芯片尺寸，- 门数量，- 金属层数量，- 与外部接口的连接方式，- 硬核 IP/宏单元 ，- 电源分配，- 多电压设计 ，- 时钟方案 ，- 扁平设计或分层设计?



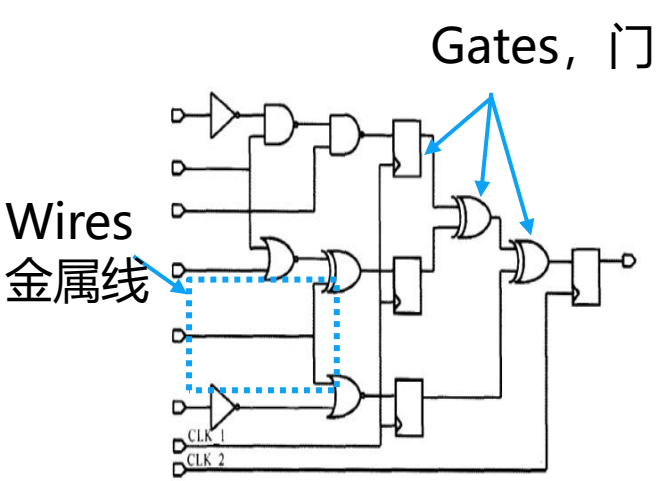


Placement（布局）

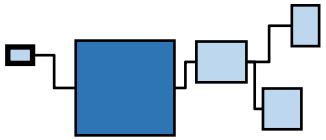
- Placement in physical design



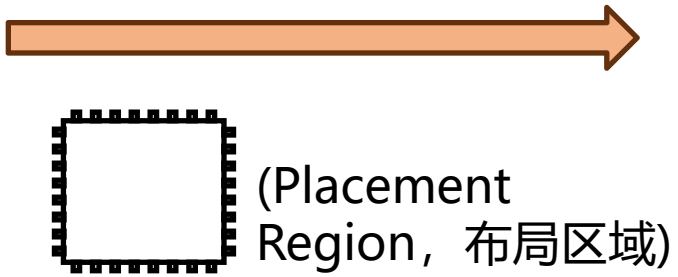
- What placement means?



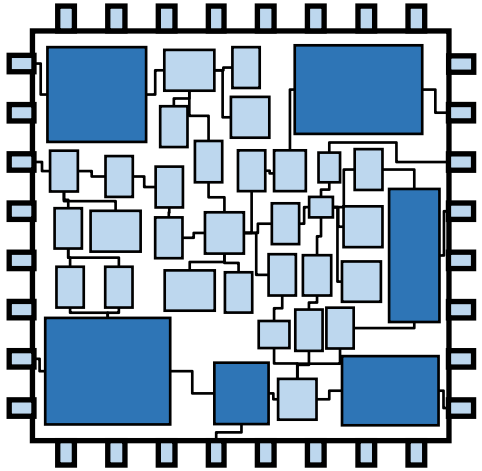
(Netlist，网表)

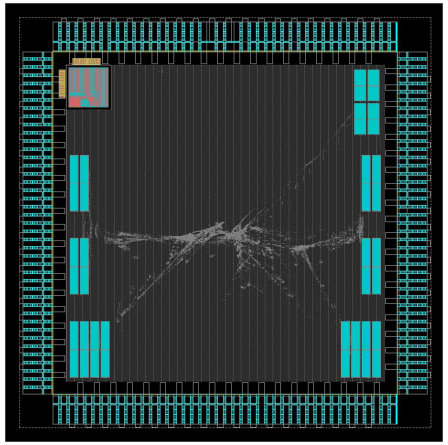


(Cells，单元； Nets，线网)



(Placement
Region，布局区域)





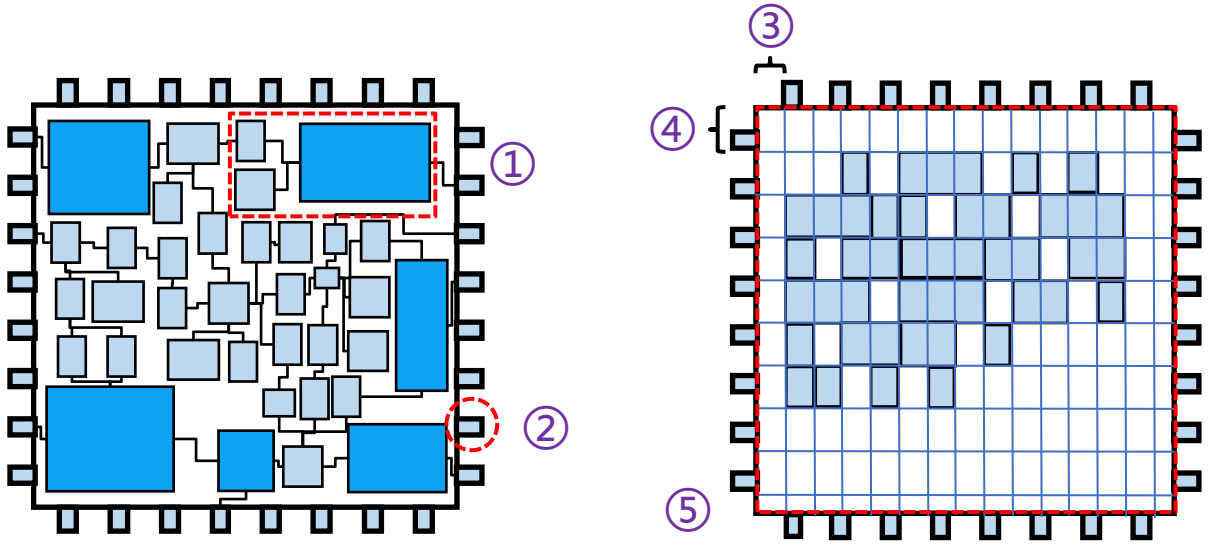
(Placement Result)

Placement（布局）

- **布局问题介绍**

给定有连接线关系（线网）的单元集合以及布局区域，布局对单元进行放置。一般布局目标是最小化线网总线长/时序/功耗，要求单元满足合法性（在布局区域内、对齐Row/Site、单元相互不重叠等）的规定。

- 线网：单条线网可连接多个Pin点（Pin点位置在单元上或者是在IO处）；线网走线方向只有横纵方向。
- 单元：形状通常是矩形。单元类型有宏单元、标准单元（时序单元、逻辑单元）等；单元状态有已固定、待放置等。



① 单元及其线网
② IO pin
③ Site（布局最小网格）
④ Row（行）
⑤ 布局区域

Clock Tree Synthesis (CTS，时钟树综合)

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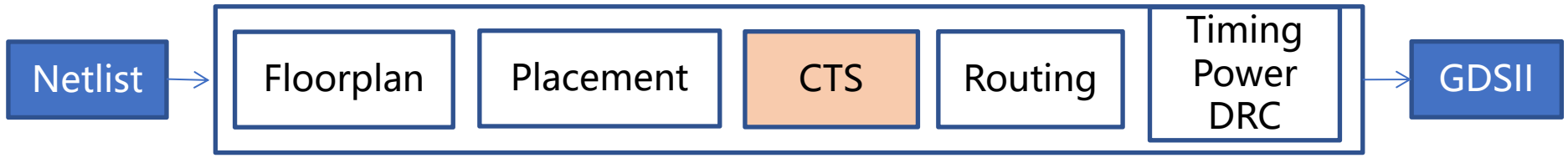
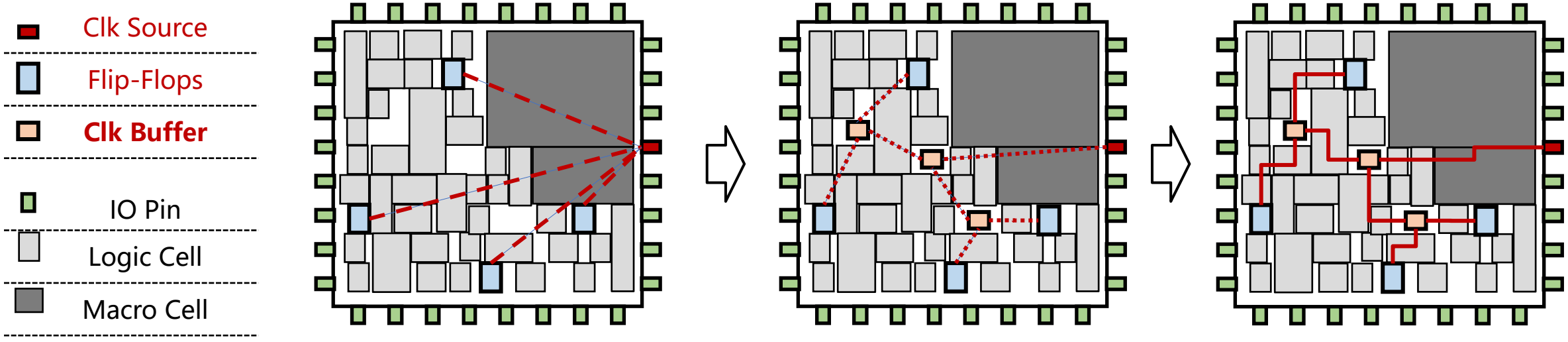
- **CTS in Physical Design**



- Achieving **skew balance** and **minimize design resource** (latency， buffers, wirelength)



Routing（布线）

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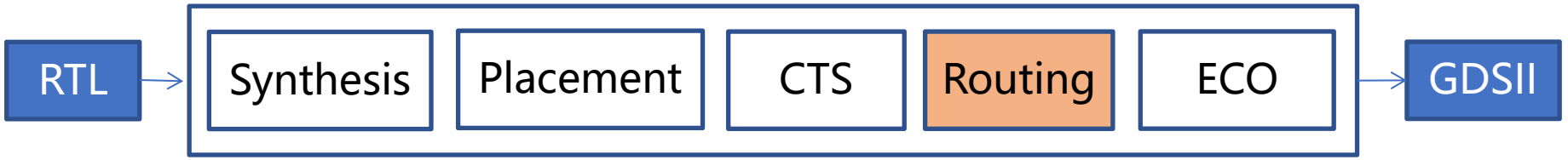
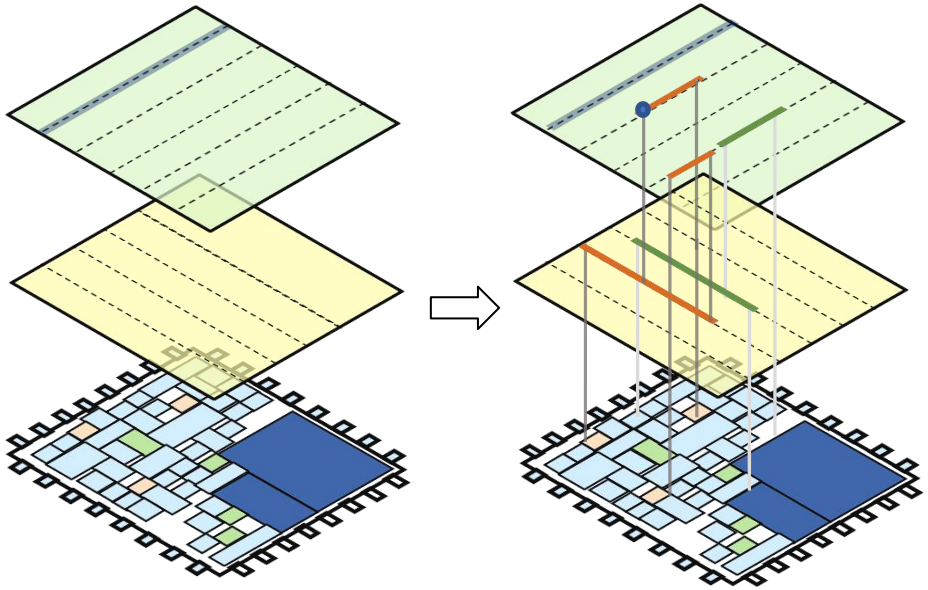
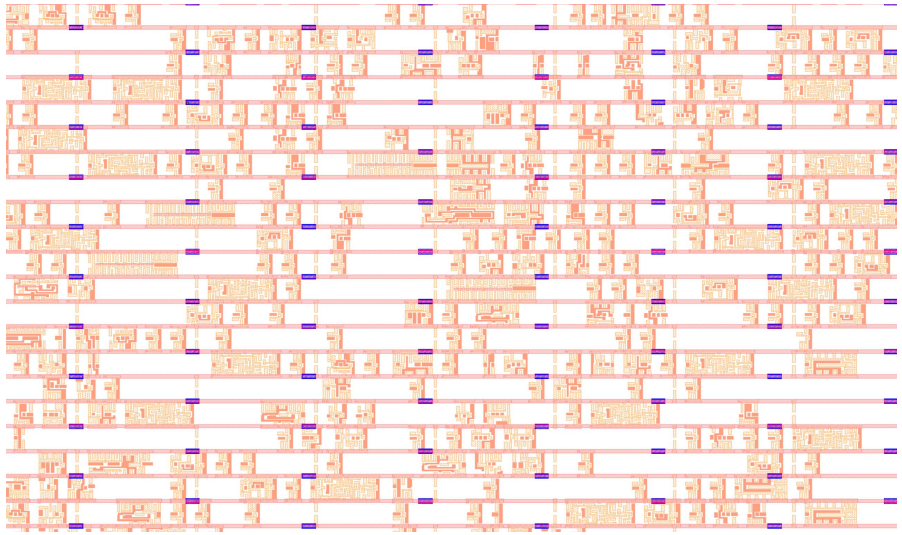
- Routing in physical design



- **全局布线：**给出每条线网net宽的、大致的布线通道，指导详细布线的进行
- **详细布线：**给出每条线网net的具体布线，到轨道上



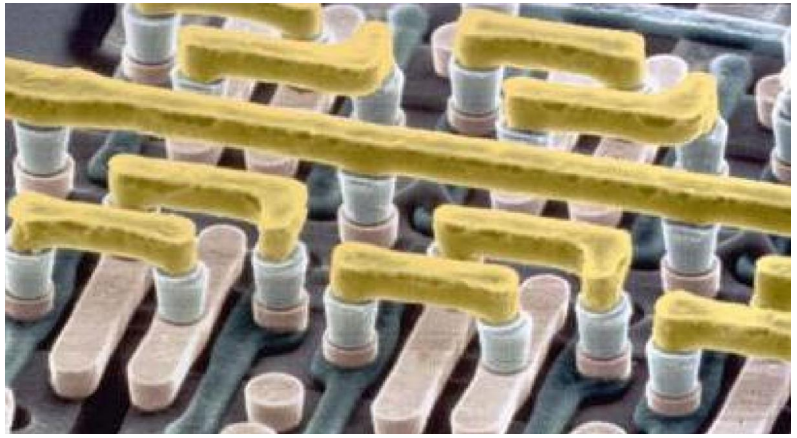


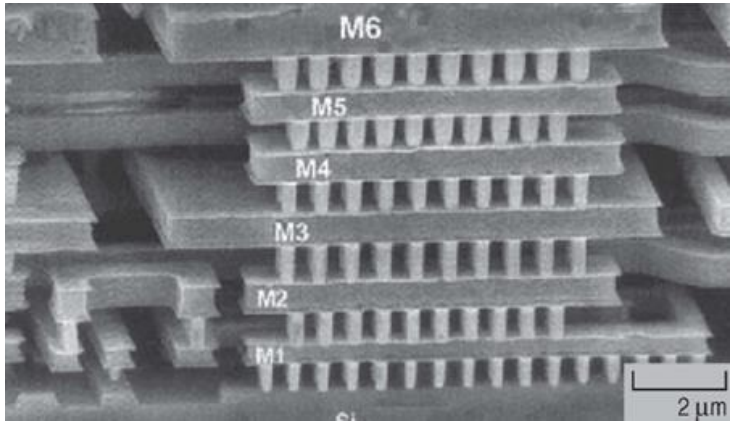
Vias（通孔）

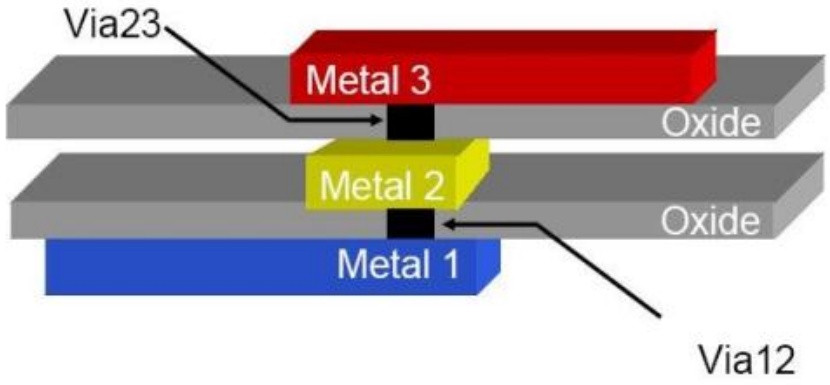
- Connecting between metal layers requires one or more vias.

Example

Connecting a signal from Metal 1 to Metal 3 requires two vias and an intermediate Metal 2 connection

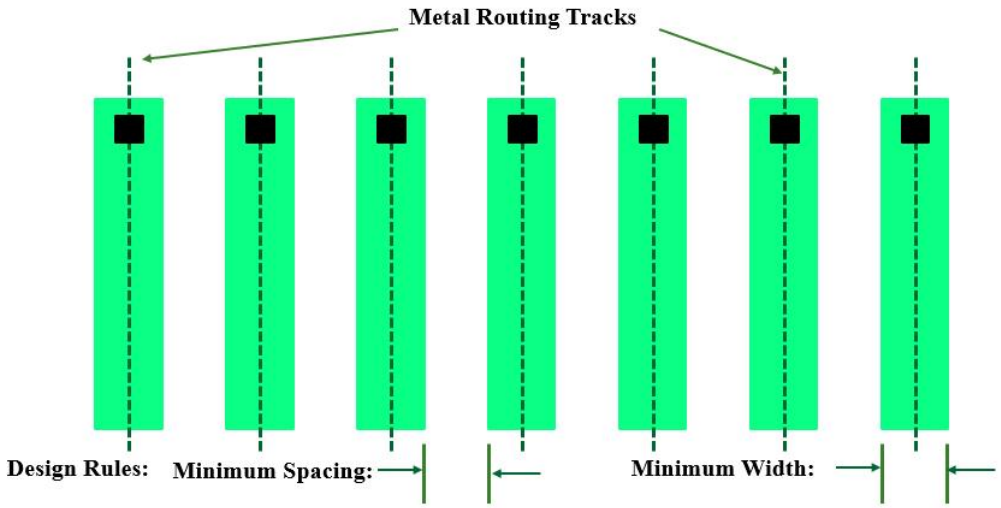






Routing Tracks（布线轨道）

- Metal routes must meet minimum width and spacing “design rules” to prevent open and short circuits during fabrication
- In gridded routers these design rules determine the minimum center-to-center distance for each metal layer, a.k.a. grid or track spacing
- Congestion occurs if there are more wires to be routed than available tracks



Preferred Routing Directions（优先布线方向）

- Metal layers have preferred routing directions
- Default preferred direction:
  - Metal 1 – Horizontal
  - Metal 2 – Vertical
  - Metal 3 – Horizontal, etc
- Why is this beneficial?

preferred routing directions

Having preferred routing directions greatly reduces the amount ofmetal layer “jumping” the router may need to do to connect anytwo pins, which reduces resistance and therefore propagation delay,as well as run time.

Conclusions

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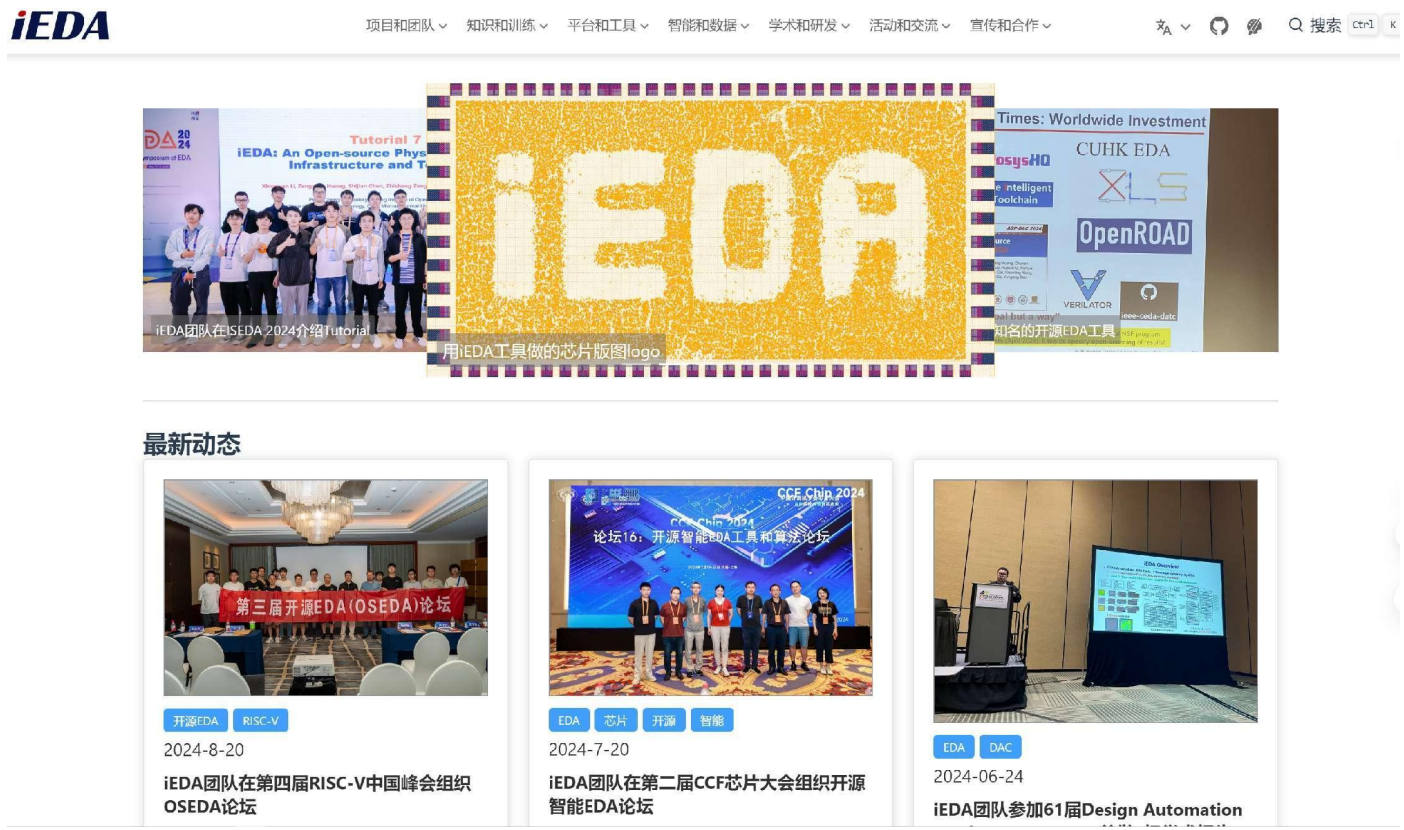
- Chip Design Flow
  - IP, Tool, PDK, Flow
- File Format
  - Verilog (Netlist), LEF/DEF, Liberty, SDC, SPEF, SDF, GDS
- Physical Design Steps
  - Floorplanning, Placement, CTS, Routing



Thanks

iEDA website: ieda.oscc.cc

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fzulxq@gmail.com